

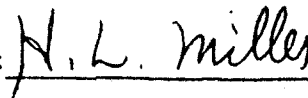
This document details the tests to be performed on the engineering model of the Solar Wind Spectrometer at the subsystem level.

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Solar Wind Experiment Test Plan

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EXPERIMENTS ENGINEERING  
TEST PLAN  
FOR THE  
SOLAR WIND EXPERIMENT  
ENGINEERING MODEL TESTS



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1.0 Scope

This plan defines the tests that will be performed by the Experiments Group on the engineering model of the Solar Wind Experiment. These tests will be performed prior to the delivery of the experiment to the System Group for use in the Array A integration tests.

2.0 Test Objectives

The objectives of the engineering model subsystem tests are to verify and demonstrate that the experiment design meets the operational and performance requirements. In addition the interface characteristics will be monitored to verify that they satisfy the requirements of IC 314104, Interface Control Specification for the Solar Wind Experiment.

3.0 Experiment Tests

3.1 Test Details

The Solar Wind Experiment has all its electronics housed within the deployed sensor package. The output data is in digital NRZ form, made up into a sequence of 186, ten-bit words. There are 16 sequences to a complete cycle of output data.

The correct functioning of the experiment will be deduced from the digital data by using the experiment test set. This may only be done by allowing the experiment to run consecutively through its operational modes and sequences. A sequence cannot be performed twice in an experiment cycle of 16 sequences, but may be held at any word and manually advanced to subsequent words.

The output data will be compared with specification limits to validate the unit. To facilitate the comparison, a master magnetic tape will be provided by JPL.

3.1.1 Power Tests

Measurements will be made of total power consumption, switch-on transient and noise on the experiment power lines. The power supply line will be monitored throughout a cycle to demonstrate that noise produced by the experiment is within the limits given in the Interface Specification. Satisfactory operation will be verified at the extremes of supply voltage level specified in the Interface Specification.



### 3.1.2 Interface Tests

The output data, timing, control and command lines will be checked for pulse shape, amplitude and noise level, using an oscilloscope camera. The results will be compared with those obtained on the Engineering Model at JPL.

### 3.1.3 Functional Tests

The experiment will be cycled and the data, which is printed in octal form by the test set printer, checked to verify correct operation. The sensor outputs will be zero plus noise. The calibration and high voltage A.C. and D.C. signals can be checked against a specification while the temperature readings may be compared with those obtained during tests at JPL.

## 3.2 Place of Tests

All tests will be conducted at Bendix Systems Division.

## 3.3 Facilities and Special Test Equipment

### 3.3.1 The Special Facilities Required Are:

3.3.1.1 Floor space to accommodate a standard equipment rack and a 2 feet by 2 feet vacuum chamber

3.3.1.2 Normal laboratory power supply 105 to 125 volts, 60 cycles per second at 30 amps.

3.3.2 The special test equipment required is either a dry nitrogen supply or a vacuum chamber. The vacuum chamber must be capable of taking the complete Solar Wind Experiment and have facilities for bringing out two cables, either direct or via connector, whichever is the more convenient. The two cables have twenty and one hundred conductors respectively. A suitable vacuum chamber will be supplied by JPL. The experiment test set is required for the engineering model tests.

#### 4.0 Test Procedure and Recording of Results

- 4.1 A test procedure, containing a test record format, will be issued for the engineering model tests.
- 4.2 The test results will be recorded and kept on file at Bendix Systems Division. Copies of the results will be forwarded to the P. I., Dr. Conway W. Snyder.

# TEST SCHEDULE FOR SOLAR WIND ENGINEERING MODEL TESTS

TASK .		TIME PERIOD DAYS											
No.	DESCRIPTION	1	2	3	4	5	6	7	8	9	10	11	12
1	TEST SET VALIDATION	←→											
2	POWER & INTERFACE TESTS		←→	→									
3	FUNCTIONAL TESTS.				←→	→							