LSG ELECTRONICS
TECHNICAL DESCRIPTION

Block Diagram - LSGE

Bxa dwng no 2365000

LSG ELECTRONICS
TECHNICAL DESCRIPTION

June 15, 1971
984-EE-~~67A~~ 99

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APPENDIX A

LUNAR SURFACE GRAVIMETER

HIGH DATA RATE

LSG ASSEMBLIES 2362181 & 2362183

Internal
Memorandum

Bendix Aerospace Systems Division

Ann Arbor, Michigan

Date 25 March, 1971 Letter No. 984-EE-83

To J. Mansour

From W. Anderson

Subject Changes in Lunar Surface Gravimeter Experiment to Implement 36 Word Format

I. Background Information

Words for the new system will be assigned as follows. All frames will have the same format.

			S		S		S
	S		S		S		S
	S		S		S		S
Tide	S	F.M.	S	Tem	S		S
	S	St1	S	St2	S		S
	S		S		S		S
	S		S		S		S
	S		S		S		S

S = Seismic
F.M. = Free Mode
St 1 = Experiment Operate Status
Tem = Temperature
St 2 = Command Counter Status

A repeating 16 state counter can be used to sequence all events within the L.S.G.E. This counter will be SYNC'ed to the frame mark pulse which occurs every 1st word in the frame. Counter states will be assigned as follows.

S	S	St1	S	St2	S		S
Tide	S	F.M.	S	Tem	S		S

The analog & digital mux will be sequenced according to this chart. Information will be loaded only with simultaneous occurance of the data gate and data demand pulses. The shift register will be loaded on the rising edge of the data gate pulse. Sequencing of counter and clearing of the analog to digital converter will occur on the falling edge of the data gate.

Each analog signal will be sampled for 118 usec. This information

must be held for 9.4 msec while A to D conversion occurs. During the slow data rate mode hold will be 18.8 msec. Error of sample & hold circuitry must be minimized.

II. Digital Multiplexer

Since data will be loaded into the output shift register on the rising edge of the data gate pulse the digital multiplexer must be set up on the falling edge of the previous data gate pulse. Sequencing of the digital multiplexer will be as follows.

S	St1	S	St2	S		S	Tide
S	F.M.	S	Tem	S		S	

To derive the control equations note that S., F.M., Tem., and Tide are all analog signals and will be denoted in the following Karnough map as A.

	00	01	11	10
00	A	St1	St2	A
01	A	∅	A	A
11	A	∅	∅	A
10	A	A	A	A

∅ = Don't Care

$A = \overline{A} + D + C$

$St\ 1 = A \cdot \overline{B} \cdot \overline{D}$

$St\ 2 = A \cdot B \cdot \overline{C} \cdot \overline{D}$

The shaft encoder control signal must over ride all digital mux inputs. Hence,

$A = (\overline{A} + D + C) \cdot \overline{Se}$

$St\ 1 = A \cdot \overline{B} \cdot \overline{D} \cdot \overline{Se}$

$St\ 2 = A \cdot B \cdot \overline{C} \cdot \overline{D} \cdot \overline{Se}$

Se = Se (Shaft encoder control)

To minimize components the following equations should be implemented.

$A = \overline{St\,1} \cdot \overline{St\,2} \cdot \overline{Se}$

$St\,1 = A \cdot \overline{B} \cdot \overline{D} \cdot \overline{Se}$

$St2 = (A \cdot B \cdot \overline{C} \cdot \overline{D}) \cdot \overline{Se}$

$Se = Se$

III Analog Multiplexer

Control of the analog multiplexer is done 2 words preceding actual data output. This is because the track and hold circuit is strobed on the preceding data gate pulse. Sequencing will occur as follows:

St1	S	St2	S		S	Tide	S
F.M	S	Tem	S		S		S

To derive the control equations ϕ states must not be overlapped.

	00	01	11	10
00	ϕ	S	S	ϕ
01	ϕ	S	S	Tide
11	ϕ	S	S	ϕ
10	F.M	S	S	Tem

$S = A$

$F.M. = \overline{A} \cdot \overline{B}$

$Tide = \overline{A} \cdot B \cdot \overline{D}$

$Tem. = \overline{A} \cdot B \cdot D$

To minimize components the following equations should be implemented.

$S = A$

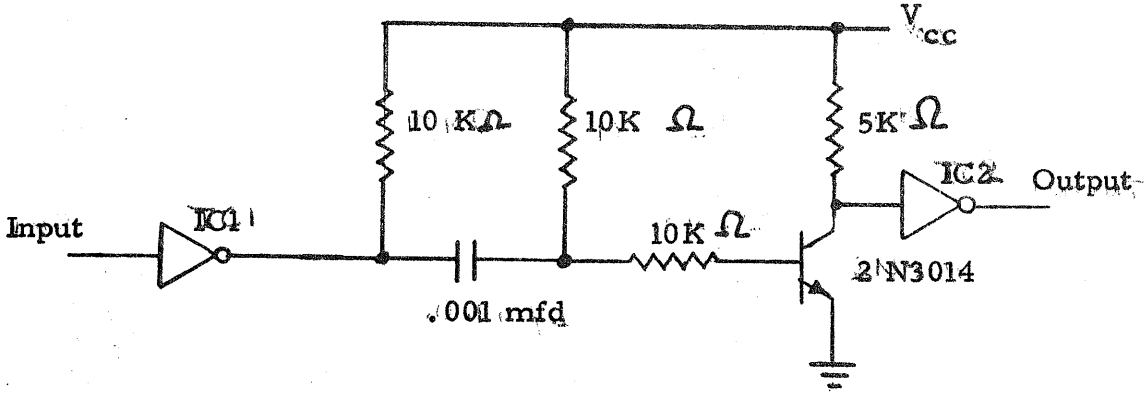
$F.M. = \overline{A} \cdot \overline{B}$

$$\text{Tem.} = \overline{A} \cdot B \cdot D$$

$$\text{Tide} = \overline{S} \cdot \overline{F.M.} \cdot \overline{\text{Tem.}}$$

IV Edge Triggers

Two edge triggers must be built in the control logic. These will sense either the falling or rising edge of a data gate pulse, depending the number of inverters used in the input.



$$I_B \text{ min} = \frac{4.5 - .8}{20\ K\Omega} = \frac{3.7}{20K} = .185 \text{ ma}$$

$$I_C \text{ max} = \frac{5.5v}{5K\Omega} + .18 \text{ ma}$$

$$= 1.1 \text{ ma} + .18 \text{ ma} = 1.28 \text{ ma}$$

$$H_{FE}\text{min} = \frac{1.28}{.18} = 7.1 \qquad H_{FE} \text{ of } 2N3014 = 12$$

5K Ω resistor could be increased, however, circuit noise immunity would also be reduced.

Consider typical time constant.

$$V_T \text{ of } 2N3014 = .6 \text{ to } .8v$$

$$V_A = \frac{5.0 - .7}{2} + .7 = 2.85v$$

Vcap with IC1 high = 2.15v

$$2.85 = 7.15 \left(1 - \epsilon^{-t/rc} \right)$$

$$5 \times 10^{-6} = .506 \times 10 \times 10^{3} \, C$$

$$C = .985 \times 10^{-9}$$

$C \simeq .001$ mfd for 5 usec output

What is max BV_{BEO} for transistor?

$$\frac{5.5 - .6}{2} + .6 = \underline{3.15} \text{ V}$$

Device is spec'd at 5v

Power dissapation for the circuit in the on condition and IC1 output low.

$$P = \left(\frac{5}{10K\Omega}\right) 5 + \left(\frac{5}{20K\Omega}\right) 5 + \left(\frac{5}{5K\Omega}\right) 5$$

$$P = 2.5 + 1.25 + 5.0 = 8.75 \text{ mw}$$

V. Sample and Hold Circuit

A. The following requirements must be met by the track and hold circuitry.

1. Zin $\geq$ 10K Ω to eliminate loading effect on driving amplifier.

2. Time to sample 118 usec

3. Time to hold = 9.4 msec (fast data rate)
= 18.8 msec (slow data rate)

4. System Error

<10mv on fast data rate
<20mv on slow data rate

5. Use NH0019 analog multiplexers

B. Sample Time

Design for 10 time constants. This will create a charge error of

$$\epsilon^{-10} = .000045$$

$$\text{Error} = \epsilon^{-10} \times 20v = .9mv$$

$$\tau = RC$$

$$11.8 \times 10^{-6} = 10 \times 10^{10}\ C$$

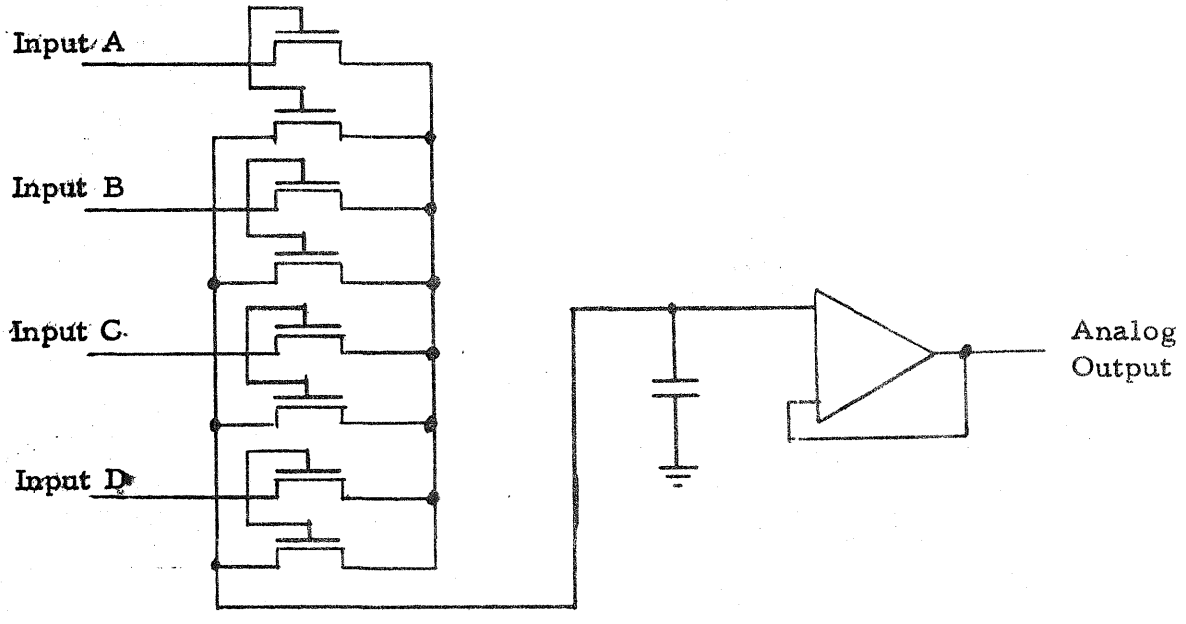
$$C = .00118 \text{ mfd}$$

C = .0012 mfd is closest standard value

Capacitor must be free of dielectric polarization. Glass will be specified for this application.

C. Hold Considerations

The NH0019 has too much output leakage under worst case specifications for this application. Hence, it will be used in the following configuration.



Typical input leakage for the NH0019 at 25°C is spec'ed at 25 pA. Our device spec. will use this limit for a maximum. Therefore, total multiplexer leakage at 25°C is given by

$$I_{leak} = 4 \times 25 = 100 \text{ pA}$$

Since FET leakage doubles for every 10°C total leakage at 55°C will be given by

$$I_{leak} = 100 \times 8 = 800 \text{ pA}$$

A Philbrick 1402-02 will be used, as the non-inverting buffer. Its' leakage is defined in data sheets as follows

ΔT = Change in temperature above 25°C

$$I_{leak} = 30 \text{ pA} + .5\text{pA } (\Delta T)$$

$$I_{leak} = 30 \text{ pA} + 15 \text{ pA} = 45\text{pA max.}$$

Total capacitor droop during a 9.4 msec hold time will be

$$Q = CV = IT$$

$$\Delta V = \frac{(845 \times 10^{-12})(9.4 \times 10^{-3})}{1.2 \times 10^{-9}}$$

$$\Delta V = 6.6 \text{ mv}$$

Total capacitor droop during 18.8 msec hold time will be

$$\Delta V = \frac{(845 \times 10^{-12})(18.8 \times 10^{-3})}{1.2 \times 10^{-9}}$$

$$\Delta V = 13.3 \text{ mv}$$

Capacitor droop is not all of the system error. Offset of the 1402-02 must also be included.

ΔT = Change in Temp. above 25°C

$$V_{off} = .3 \text{ mv} + \Delta T\ (.01 \times 10^{-3})$$

$$V_{off} = .3 \text{ mv} + .3\text{mv} = .6 \text{ mv}$$

Total System error will be

$V_{error} = .6 + 6.6 + .9 = 8.1$ mv fast data rate

$V_{error} = .6 + 13.3 + .9 = 14.8$ mv slow data rate

This meets the design criteria as now known and specified.

Input rise time to 1402-02. Fastest slope can be approximated by:

$CV = IT$ Let $\Delta V = 1V$

$I = 20/10K = 2$ ma

$\Delta T = (1.2 \times 10^{-9})\ (1)\ /\ 2 \times 10^{-3}$

$\Delta T = .6 \times 10^{-6}$

Slew rate $= \frac{1}{.6 \times 10^{-6}} = \frac{x}{1 \times 10^{-6}} = 1.67$ v/us

Slew rate of 1402 is $\geq$ 3V/u sec.

Hence, system is not limited by op. amp. slew rate.

W. Anderson

WA/dt

cc: K. Hsi
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SECTION 1

LUNAR SURFACE GRAVIMETER EXPERIMENT

1.1 EXPERIMENT OBJECTIVES

The lunar surface gravimeter experiment is designed to gather information on the following relatively independent areas:

i) Absolute lunar gravity

ii) Tidal changes in local gravity due to the change in relative position of celestial bodies (moon, earth, sun and others)

iii) Low level lunar gravity changes with periods between 10 secs to 20 mins due to natural oscillations of the moon.

iv) Vertical axis seismic activity

The vertical component of gravity is detected and measured at three different frequency spectrums. These are the tidal (DC to .008 HZ), free modes (.0008 HZ to .12 HZ), and seismic (.05 to 2 HZ). These signals are detected with an accuracy of one part in one thousand with the following resolution levels: 2μgals for the tidal signal, $.008\mu$gal for the free-modes signal and .0001 microns for the seismic signal. From the information gathered conclusions may be drawn about:

i) The internal constitution of the moon

ii) Seismic activity in the moon which is detected both on the seismic and the free-modes channel

iii) The signal on the free mode channel may also come from the normal modes of oscillations of the moon which may be caused both by seismic activity and gravitational waves if they are of sufficient intensity and are in the appropriate frequency spectrum. These excitation source may be shown to be due to gravitational waves by correlating with measurements made simultaneously on earth.

1.2 SYSTEM DESCRIPTION

The gravimeter sensor is an adaptation of the basic LaCoste and Romberg geodetic gravity field meter. It consists of a beam, sensor mass and a zero-length spring with the beam arranged to pivot at a point by a suspension arrangement. The sensor is designed so that the spring is attached to the center of gravity of the mass and the beam. The quiescent operation of the system is determined by the length of the spring which could be adjusted by moving the point to which the other end of the spring is mounted by means of a screw. The screw position is detected by a shaft encoder to which it is mechanically coupled. This screw position is calibrated on earth and therefore provides information on the lunar absoulte g with an accuracy approaching the accuracy known on earth.

Calibration of the instrument is done on earth and therfore the sensor has to be capable of operating on earth within the range of the sensor spring and screw. This capability is provided by the mass changing mechanism. The sensor may be operated with a smaller mass to accomodate the larger gravity on earth. Also since the lunar gravity is known only to an accuracy of 1%, themass changing mechanism has the capability of trimming the lunar mass with two smaller masses.

The deflection of the beam from its quiescent operation to an acceleration force is dependent upon the tilt of the beam with respect to the local horizontal. Adjustment of the beam tilt is provided in the experiment for proper operation.

The sensor spring constant is affected by temperature and has a minimum spring constant at its 'spring inversion temperature". It is at this point where the spring constant is least sensitive to temperature changes and therefore the sensor is operated near or at this temperature. To minimize the variation of the spring constant due to temperature and retain the required accuracy of the sensor, a temperature controller is provided to maintain the temperature to $\pm .001^{\circ}$C over an hour and $\pm .01^{\circ}$C over one month. The actual temperature is monitored to detect and thus make corrections for possible long term temperature drifts over $\pm .01^{\circ}$C. The controller is designed to operate at different temperature increments around the expected spring inversion temperature so that the sensor may be operated close to or at the spring inversion temperature. This provision also enables experimental determination of the actual spring inversion temperature.

The deflection of the beam is detected by a differential capacitor

whose center plate is attached to the beam. The differential capacitor is driven by a balanced A-C signal. The magnitude and phase of the suppressed carrier signal from the center plate indicates the position of the beam from center. This A-C signal is amplified and converted to a D-C signal by a series of amplifiers and a demodulator. The post amplifier has 16 gain steps to accomodate the large signals during the initialization of the experiment and to provide adjustment of the transient response of the system.

The demodulator output is passed through a low gain amplifier to detect large deflections of the beam during the initialization of the experiment to establish the quiescent operation of the spring.

In order to operate the sensor over a wide range of gravity change, a feedback voltage applied to the capacitor plates balances the force due to gravity change and brings the beam back to near its center position (A-C null). The restoring force is obtained by modulating a constant voltage bias across the capacitor plate. The electrostatic force generated is directly proportional to the feedback voltage which is obtained by integrating the beam position signal from the demodulator. Thus for sufficiently low frequency (tidal and free-modes signal) such that the integrator has enough time to follow, the integrator output is directly proportional to gravity change. The output of the integrator for the tidal signal is of adequate amplitude and its output provides the tidal information. The free-modes signal however are at a much lower intensity and the integrator output is further amplified and filtered.

The seismic signals are of higher frequency than the tidal or free-modes signal. These signals are at a frequency range above the natural frequency of the sensor mass-spring, that is the beam remains fixed in space because of its inertia. The seismic signals are therefore detected by the motion of the fixed capacitor plates relative to the beam. The signals are of low level and a second amplifier is provided to amplify and filter the demodulator output.

SECTION 2

LSG ASSEMBLY 2362171

2.1 DIGITAL MUX CONTROL CIRCUIT (Low Data Rate)

2.1.1 General Description

The function of the digital MUX control circuit is to channel scientific data from the Analog to Digital converter, Experiment Status information, and Shaft Encoder information with LSG telemetry format.

Experiment and Command Status are transmitted on every 15th frame. The gating is accomplished by a 15th frame counter and associated control logic. Every 15th frame, the Tide and Free Modes data assigned to telemetry words 13 and 15, are inhibited and status data are transmitted in their place.

During the shaft encoder "on" mode, all other signals to the digital MUX are inhibited and the shaft encoder signals are fed in. Gates are used to make the transfer.

A final function of the circuit is to steer, load, and shift out pulses for the digital MUX control.

2.1.2 Circuit Description

The count of fifteen circuit is comprised of 4 stage counter U16. The U16 Q outputs gate input terminals 6, 8, 9 and 7 of 14B which decode the count sixteen from the counter refer to schematic 2362054, sheet 1. As soon as the count of sixteen is received, the output terminal (10) goes to zero thus causing terminal 3 of U17 to go to one, thus resetting the counter to the zero state. The counter is also reset to zero by the 90th frame pulse via pins 6, 7, 5, 1, and 3 of U17. Capacitors C4 and C5 provide a small amount of delay in the reset path so that effects of false or intermediate states are removed. There is one minor drawback to this type of counter in that the count of 15 state does not end exactly at the count of 16 trigger but extends slightly into the count of 16 period. However, this delay is short and causes no problems.

The count of 15 is decoded by a gate (output 2) of U14. One inverter of U12 inverts the least significant bit and applies it to input 12 of U15 thus giving the required code.

The three gates of U15 are used to generate enabling signals for the Digital MUX Control. These gates perform a NAND function to decode the 15th frame count for generating the experiment operate and command counter status functions and the shaft encoder enable function. The resultant signals are status enabling functions for gating the digital MUX. Shaft encoder control is inverted via U11A and U12A and applied directly to the digital MUX as the enabling signal. This signal is also applied as a disabling signal to all three gates of U15 thus disabling Experiment Status, 1 & 2 and the A-D Enable function outputs during transmission of shaft encoder information.

One gate of U15 (output 3) receives the positive going (inverted) count of 15, the positive shaft encoder control and the positive going (inverted) experiment status No. 1 signal at its input terminals. When all three inputs are positive, the gate output goes negative. This signal is inverted by U11B & C and applied to the digital MUX as an experiment status enable function.

Similarly, another gate (output 13, U15) has positive going 15 frame, positive going Exper Status No. 2 and positive shaft encoder control applied to the inputs. When these inputs are all high, the gate output is low. This inverter signal is applied to the digital MUX as Exper Status No. 2 enable.

The third gate of U15 has the outputs of the other two gates connected to two inputs, and the shaft encoder control connected to the third input. The gate output will be low when shaft encoder control, or Experiment Status No. 1 or 2 enable are low. This output is inverted and applied as an A-D Enable signal which is present at all times when the other signals are absent.

Load and Shift pulses for the digital MUX are generated by gating the data gate and inverted data demand signals together (pins 12, 13 and 14 of U17B). Load pulses appear at the output in response to the data gate immediately after the trailing edge of the data demand pulse. This causes the digital MUX shift register to be loaded during any word except one in which data is transmitted.

Shift Out pulses are generated by gating the clock and data demand signals together (pins 1, 2 and 3 of U10). The resultant shift pulses appear at the clock time, period and width but occur during the data demand only. Thus, a block of ten shift pulses appear during each data demand and empties the digital MUX shift register at the clock rate.

2.2 DIGITAL MULTIPLEXER

2.2.1 General Description

The digital multiplexer is a data selector. It is used to select one out of four data sources. The four data sources are one analog to digital conversion word, two Experiment status words and one shaft encoder word. In general, according to application, digital multiplexers can be designed to perform one of four possible functions, i.e., serial in-serial out, serial in-parallel out, parallel in-serial out and parallel in-parallel out. For LSG application, the digital multiplexer is designed to function as a parallel to serial converter.

2.2.2 Principles of Operation

The digital multiplexer is comprised of ten, 4-wide 3-2-2-3 input AND-OR-INV gates and a 10-bit right shift register. Upon activation by one of the four enable lines, a desired 10-bit word is entered into the ten 'EXCLUSIVE OR' gates. Upon the command 'LOAD' the same word is loaded into the right shift register from the outputs of the exclusive-or gates. Finally upon receiving the SHIFT command, the word is shifted serially at the output of the digital multiplexer.

In the ALSEP data format, the word assignments are 11, 13, 15, 43 and 47 are for the LSG experiment data transmission. In the electrostatic mode, in each 14 frames, the scientific data are sampled with these five words. However, every 15th frame words 13 and 15 are used for transmitting Experiment status data.

After the Screw Servo mode of operation has been completed, the shaft encoder control line is activated when the 90th Frame occurs after the 'READ SHAFT ENCODER' command is sent. The shaft encoder status will be readed out with the CORSE first and the FINE next. The sequence of data shift is the MSB first and the LSB last. The Shaft Encoder operational mode will continue for 90 ALSEP Main Frames. Table 2-1 shows the five words assigned to the LSG experiment and the three main telemetry modes of the experiment. Figure 2-2 shows the timing relation between DATA DEMAND, LOAD SHIFT and SERIAL OUT for an assumed digital word of 1011001001. The data demand pulse width is 9.4 ms. Its leading edge leads the shift pulse leading edge by 236 us. At the trailing edge of data demand pulse, a positive going 118 us pulse is used to load data in parallel into the 10-bit shift register. In the electrostatic mode, the digitized scientific data or engineering status is available at the inputs of the digital multiplexer 236 us

before the LOAD pulse. In the screw servo mode, the shaft encoder status bits should be settled at the inputs of the digital multiplexer 25 us before the LOAD pulse. The word which loaded in at the trailing edge of the first data demand pulse will be shifted out at the serial output in the second demand pulse.

2.2.3 Functional Diagram, Interface Signal Requirement

The functional diagram of the digital multiplexer is shown in Fig. 2-4. The waveforms for the enable line signals are shown in Figure 2-3. The characteristic of all input and output pulses are:

Amplitude	-	high level	+2.5 v to 5.5 v
	-	low level	0 v to 0.4 v
Rise and Fall Time			<10 us

2.2.4 Integrated Circuits Description

The digital multiplexer consists of ten exclusive-or gates (SN54L54T) wired parallelly and three 4-bit shift registers wire serially to make a 10-bit right shift register. The principles of operation of these devices are given as follows:

a) SN54L54T: SN54L54T is a low power 4-wide 3-2-2-3 input AND-OR-INV gates, upon activation by one of the four enable lines, a desired data bit is selected and transferred to the output of the device. Therefore, 10 devices will present a desired word to the inputs of the 10-bit right shift register.

b) SN54L95T: In the LSG experiment, three low power SN54L95T are wired to be a 10-bit parallel load in and right serial shift out register. Pin 6 and 8 of this device are connected to the LOAD line. At the leading edge of LOAD pulse, the data bits at the inputs are loaded to the Q side of their respective flip-flops. Pin 7 is connected to the SHIFT line. Upon the leading edge of shift pulse (236 us after the leading edge of next data demand pulse) the stored 10-bit data begins to shift out at the rate of 940 us per bit.

TABLE 2-1

LSG EXPERIMENT TELEMETRY OPERATIONAL MODES

Mode	Word Assignments				
	11	13	15	43	47
A/D Enable Frames 1-14, 16-29, 31-44 46-59, 61-74, 76-89	Seismic	Tide	Free Mode	Seismic	Temp
Exper. & Command Status (every 15th frame)	Seismic	Exper. Status	Exper. & CMD Status	Seismic	Temp
Shaft Encoder Enable. Repeated for 90 Frames	Coarse Screw 9 MSB	Coarse Screw 10 LSB	Fine Screw 9 MSB	Fine Screw 10 LSB	Coarse Screw 9 MSB

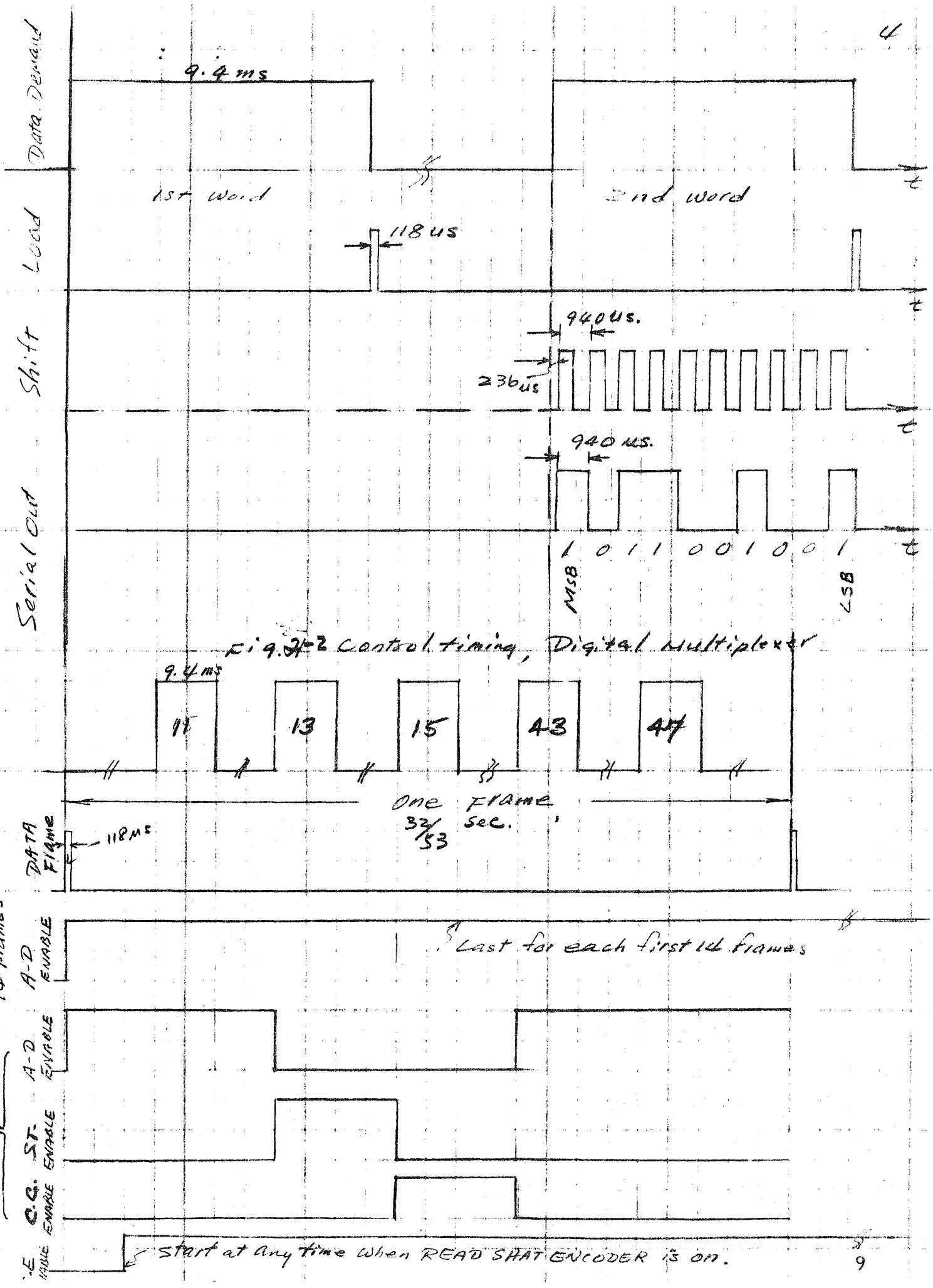


Fig. 9.2-2 Control timing, Digital Multiplexer

SECTION 3

LSG ASSEMBLY 2362172

3.0 COMMAND DECODER, COUNTER, & DIGITAL BUFFERS

3.1 General Description

Functions accomplished on this board are the buffering of all digital signals to and from the Central Station, command counting, decoding, and relay driving of gravimeter commands, and processing of all ALSEP direct commands.

Buffering of all digital signals to the Central station is performed in order to meet the requirements that digital interface lines have only one load, that capacitors be placed in all receiving and transmitting lines, and that resistors be placed in series with transmitting lines.

To insure proper operation the data gate is delayed on this board by transmission through several gates.

Direct Central station commands such as command decoder power on-off, and heater power on and off are inverted by gates and passed to relay drivers, which activate remote latching relays.

The command counter is a five stage reversible counter which responds to "Command Up", "Command Down", "Execute", and "Reset". The counter moves one step upon receipt of a central station command "Up" or Command "Down". A total of 32 positions are available. Reset of the counter is accomplished automatically when the command decoder "on" command is received.

Two MSI chips, each capable of 16 commands are used to decode the five bit states of the command counter into 32 output command lines. Decoder outputs are used directly where logic commands are needed; relay drive signals are inverted by gates which inturn drive the relay drivers.

3.2 Circuit Description

Digital control signals buffered by the unit pass through two gates so that they are not inverted. Input signals have a 1000 PF capacitor across the line, the experiment output signal, (digital MUX out) has a 330 OHM

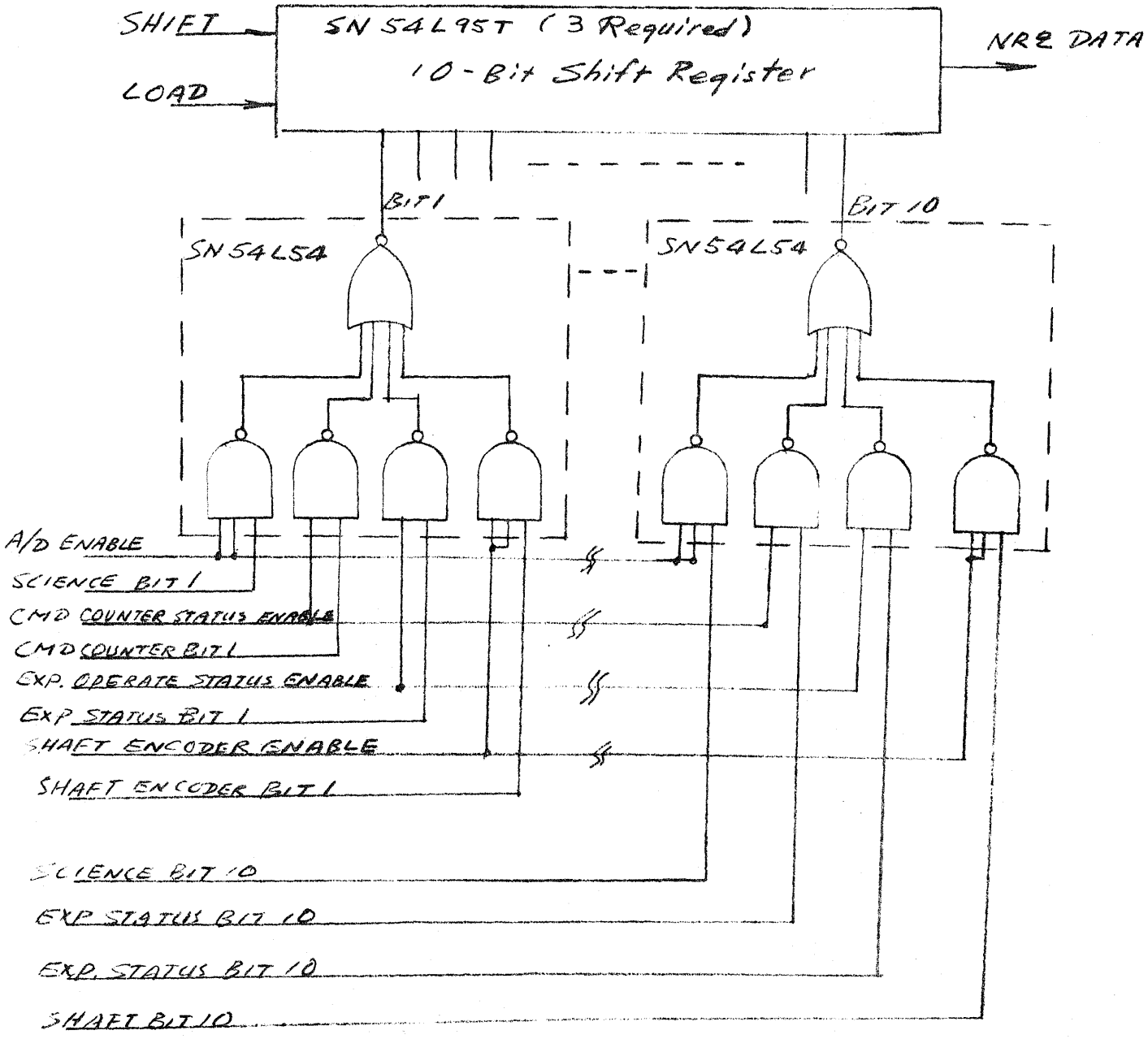


Figure 2-4 Functional Diagram, Digital Multiplexer

resistor in series with the line and a 1000 PF capacitor across the line. The data gate signal is passed through six gates in order to achieve extra delay.

The instrument heater on-off and command decoder power on-off signals are passed through gates and then relay drivers.

Command count "up" command count "down" and command "execute" are buffered by two inverting gates. Command "up" and command "down" are then applied to a set-reset flip flop made from two gates of U4 (14 and 8 outputs). Refer to 2362085 Therefore, as soon as the command "up" or "down" is received the flip flop is set into the appropriate state. An output of the flip flop, (pin 8) is connected to the four inputs of exclusive OR gate U8 which is used to reverse the counter.

Command "up" and 'down" signals are (OR'd) in a gate of U8 (output pin 3). The resultant output is used as the counter clock and is applied to counter modules U1 , U 2 and U 3.

One section of U-1 (output-pin 13) operates as a simple divide by two circuit with output, bit 1. Bit 1 drives one section of Exclusive OR U8 (pin 2). The output of this section of U8 in turn is applied to the J, K, inputs of the second section of U1 . When these inputs are high, the flip flop toggles, when low, the clock causes no change of state. Since the clock toggles this flip flop only every other time, the resultant output (Bit 2) has a frequency division of four. Furthermore, the direction of count is reversed by the up or down signal at the exclusive OR input.

Bit 2 drives one input of the second exclusive OR section (pin 5 of U8). The output of this section is 'anded' in one section of U- 9 with the output of exclusive OR #1, inverted, and applied to the J, -K inputs of the third flip flop (U 2). Again, this flip flop toggles only when the J-K inputs are high. Since the gating allows this to occur only during one period of the already established count of four, the flip flop output is a count 8, (bit 4). The direction of count is again inverted by the directional signal at the exclusive OR input.

Bit 4 is connected to the input of the third exclusive OR, the output of which is "anded" with the same signal which controls the J-K inputs of #3 flip flop. The output of the gate is inverted and connected to the J-K inputs of flip-flop #4 (second section U- 2). Since these inputs become

high only when Bits 1, 2, and 4 become high, (or low, depending on count direction) the flip flop can toggle only during 1/4 of the clock periods and this becomes a count of eight. The output of the flip flop (bit 8) is connected to the fourth exclusive OR. This output is "anded" with the signal driving the J-K inputs of flip flop #4, inverted and applied to the J-K inputs of flip flop #5. Since this signal becomes high only when all preceding outputs are high (or low), the stage toggles 1/8 of the time and becomes a count of sixteen.

The counter outputs are connected to the inputs of two decoder modules. Each decoder module decodes four binary input bits into a parallel 16 line output. Bit 16 enables one decoder module, bit $\overline{16}$ enables the other decoder module. Thus a total of five input bits gives a 32 line output.

Logic command outputs going to the various commanded areas are taken as negative going signals directly from the decoder outputs. Relay commands are inverted by applied to the inputs of relay drivers circuits. The relay drivers provide on and off signals for latching relays located at various points in the gravimeter. Each relay driver can actuate up to three relay coils. However, in the present system design each driver operates only one coil.

The command "execute" signal is buffered by two gates and applied as an enabling signal to the 16 wd decoder modules, thus sending out the selected command for the 20 millisecond period that the execute command is given.

Pressure transducer "on" command is given as one of the 32 command counter commands. Pressure transducer "off" command is obtained by transmitting the All Motors Off command.

The Command Decoder power on command provides two functions; (i.e. provides +5V power to the command decoder circuit, and resets the command counter.) It should be noted that this command can be repeated whenever it is desired to reset the command counter.

SECTION 4

LSG ASSEMBLY 2362173

4.1 ANALOG MULTIPLEXER (Low Data Rate)

4.1.1 General Description

The Analog Multiplexer is used to select one of four scientific signals to the input of the analog to digital converter so that it can be digitized in the A-D converter. The analog gates are designed to turn on for a period of one word length and time distance between one word and the next word. However the voltage digitized is the voltage presented by the gate in the period of word length, the voltage which presented in the time between two consecutive words will never be digitized since witnout having the DATA DEMAND pulse there will be no 'clock' to the register in the A-D converter even the ALSEP clock is available.

The analog multiplexer consists of two SN54L95T, one SN54L00T, two NH0019A s. The functions of these components are listed as follows:

Components	Functions
SN54L95T	5-bit right shift register
SN54L00T	NAND
NH0019A	Analog FET Gate & Voltage translator

4.1.2 Principles of Operation

The word positions assigned for LSGE are 11, 13, 15, 43, and 47. Fig. 4-1 indicates how the four scientific data measurements are digitized and transmitted for the corresponding LSG word assignments.

Referring to Dwg. No. 2362059. The Frame Mark pulse, initializes the 5-Bit Shift Register to the 10000 State via U2-13, U2-12, U2-10, U2-9, U3-13 Then for each Data Demand pulse, the bit '1' is shifted sequentially from U2-13 to U2-12, U2-12 to U2-10, U2-10 to U2-9, U2-9 to U3-13, and U3-13 back to U2-13. The following matrix shows the shift of '1' in one frame.

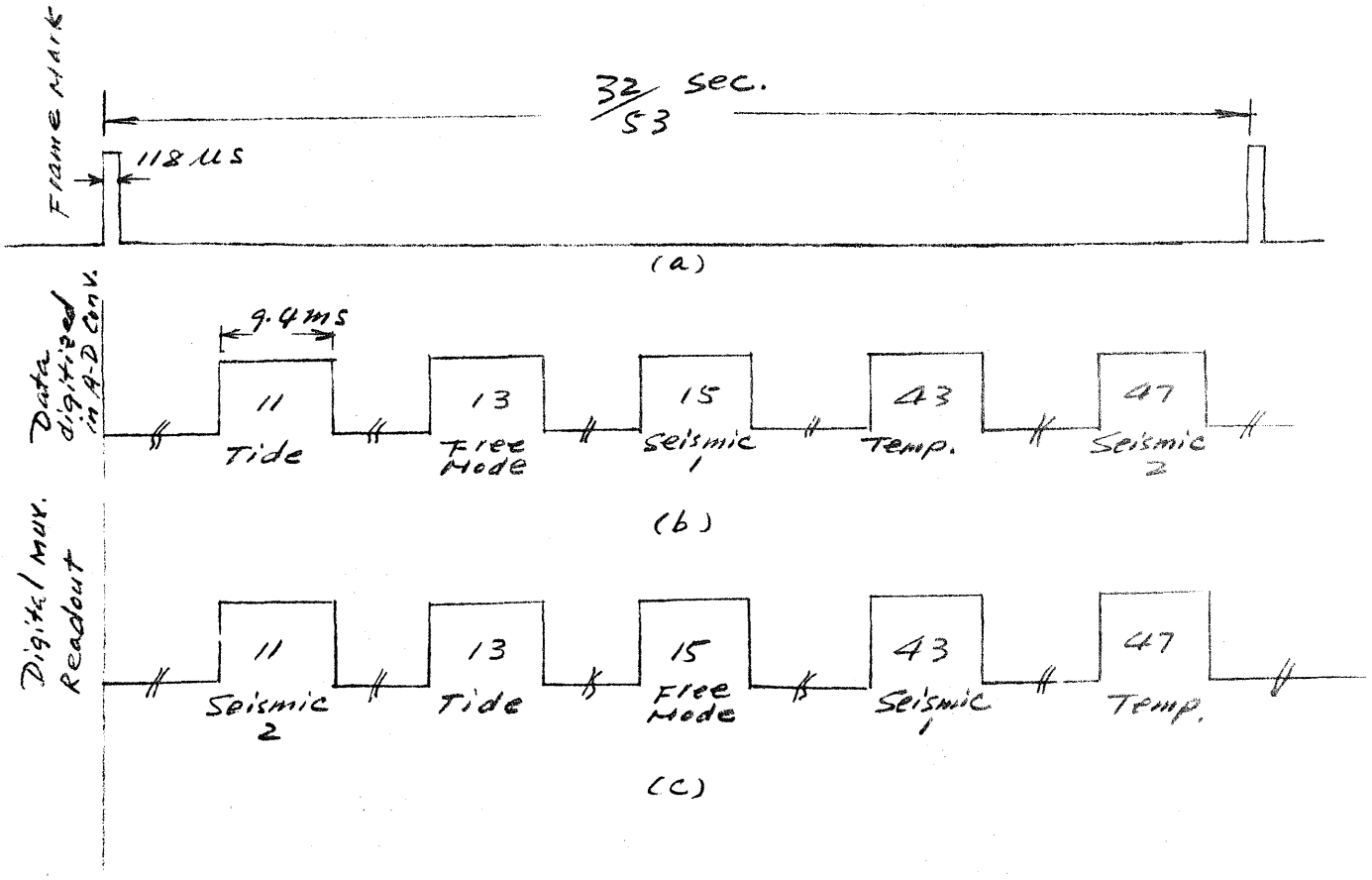


Figure 4-1 Word Assignment for Four Scientific Data

	U2-13	U2-12	U2-10	U2-9	U3-13
Frame Mark	1	0	0	0	0
W. 11 - 1st Data Demand	0	1	0	0	0
W. 13 - 2nd " "	0	0	1	0	0
W. 15 - 3rd " "	0	0	0	1	0
W. 43 - 4th " "	0	0	0	0	1
W. 47 - 5th " "	1	0	0	0	0

It can be seen from Fig. 4-1 (b) and 4-1 (c) that the time of readout a digitized signal is always one word lagging by the time it is digitized. The following list shows that both the sampling and readout for the seismic signal are designed in equal word distance basis.

Sample	Seismic 2 to Seismic 1	Seismic 1 to Seismic 2
Word Dist.	47 - 15 = 32	15 + 64 - 47 = 32
Readout	Seismic 1 to Seismic 1	Seismic 2 to Seismic 1
Word Dist.	43 - 11 = 32	11 + 64 - 43 = 32

In every 15th frame of the electrostatic mode, words 11 and 43 are remained with seismic sampling. The word 13 is to be used for readout of engineering status bit 1 to bit 10 and the word 15 for readout of engineering status bit 11 to bit 20. (The last 5-Bits are command counter status.)

4.1.3 5-Bit Shift Register

Two SN54L95T are connected as shown in Fig. 4-2 to make up the 5-Bit Shift Register. An SN54L95T shift register is composed of four R-S master-slave flip-flops, four AND-OR-INV gates, one AND-OR gate and six inverter-driver. When state '1' is applied to the mode control and pin 8, the number 1 AND gates are inhibited and the number 2 AND gates are enabled to allow entry of data through parallel inputs A through D. This mode permits parallel loading of the register. When state '0' is applied to the mode control and a clock is applied to pin 7, the register will shift one step right for each clock pulse.

FIGURE 4-2 5-BIT SHIFT REGISTER

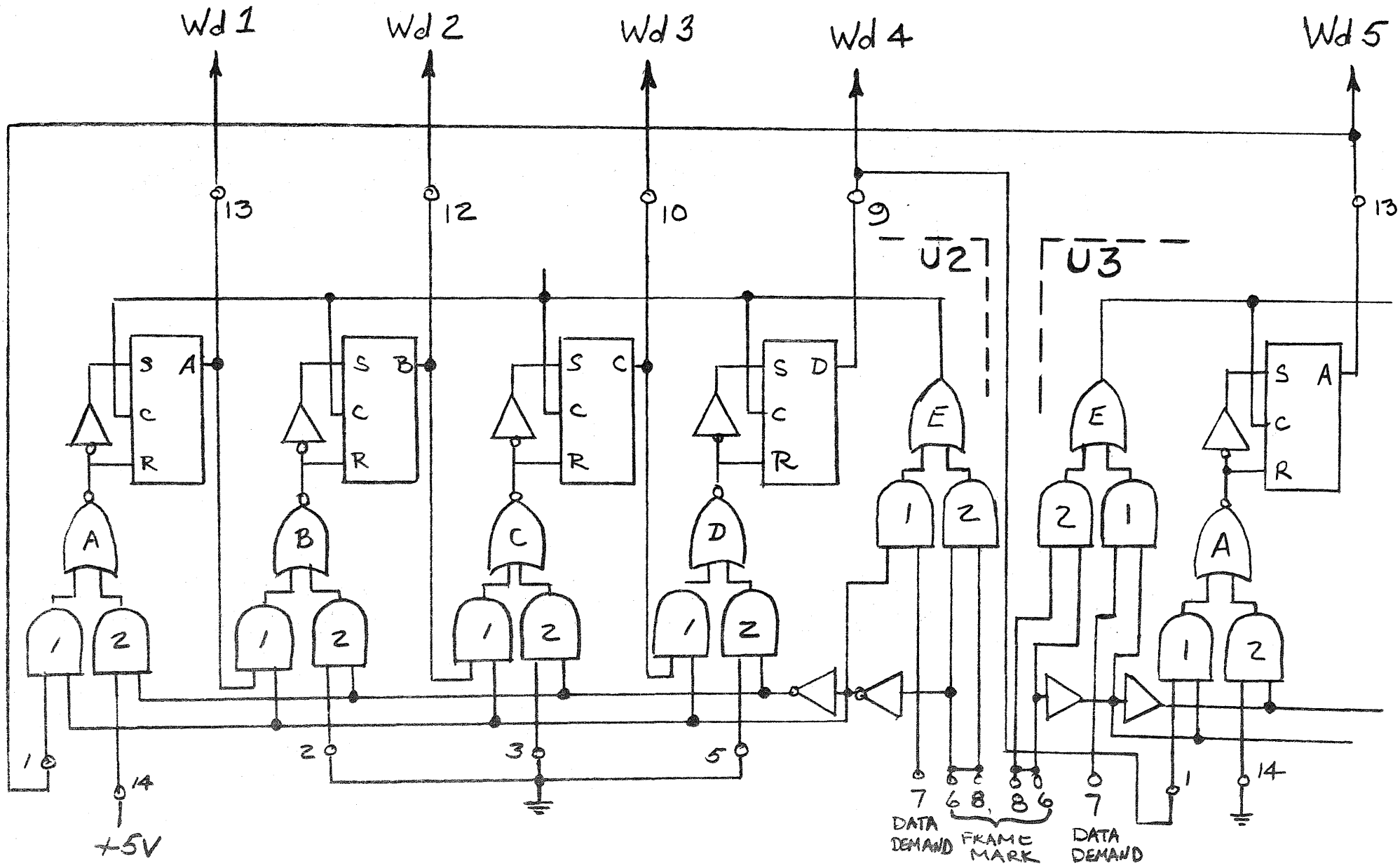
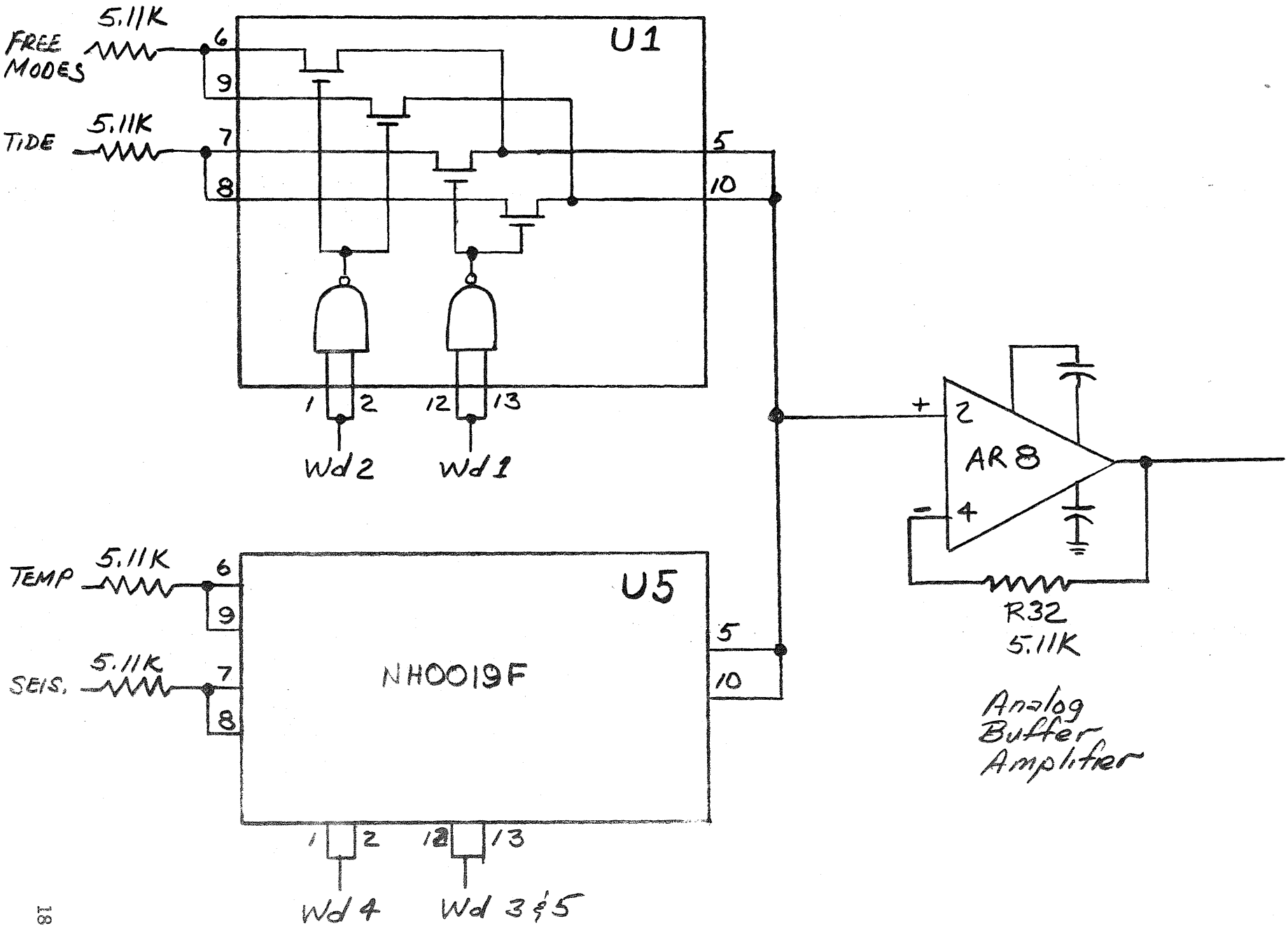


FIGURE 4-3 ANALOG MULTIPLEXER & BUFFER AMP.



4.1.4 Analog Multiplexer

The Analog Multiplexer is comprised of two NH0019F 2-channel MOS switches (refer to Figure 4-3). The NH0019F has a self-contained voltage translator, thus providing the interface required between TTL 5 volt logic and MOS FET device.

The Analog Mux is driven directly by the 5-Bit Shift Register.

4.1.5 Analog Buffer Amplifier

Refer to Figure 4-3. The Analog Buffer Amplifier (AR8) provides the appropriate signal conditioning prior to performing the A/D conversion. The Buffer Amplifier is set for unity gain as determined by the feedback resistor R32 and the 5 ,11K resistor(s) at the input of the analog multiplexer.

The gain determining resistors serve a dual function. The slewing rate of AR8 (NH0001A) is not fast enough with respect to the switching speed of the Analog Mux. Therefore, large voltage differentials between sampled data channels (e. g. +10V to -10V) will damage the Op Amp. The 5.11K resistors in the input of the Op Amp serve as limiting resistors to protect the amplifier.

Because of the turn-on/turn-off storage times inherent to the MOS FET, a momentary cross-over condition exists between switching channels. This in effect, allows a momentary shorting of input signals (Tide, Free Modes, Seismic and Temp). The 5.11K resistors at the input to each channel serve as limiting resistors; thus preventing possible circuit damage and preserving the integrity of the science data.

4.2 ANALOG OUTPUT BUFFERS

4.2.1 General Description

Ten data lines are provided to transmit selected analog data to the ALSEP Station. The ten selected data are normally at different voltage levels. Among them, seismic, Tide, Free Mode, Temperature are in the range of -10V to +10V. The a. c. oscillator amplitude is 7V peak to peak, pressure is in the range of 0 to 5V. Mass position signal is in the range of -6V to 0V. The three power supply voltages are +15V, -15V and +5V. These analog data are processed through either a buffer and level shifting network or a resistive divider to convert them either to a 0 to +5 volt range, or to a 0 to +2.5V range. The ALSEP station samples

these data once every 90 frames and digitizes it to a 8-bit binary code. The resolution of the analog to digital conversion is 19.7 mv per binary state.

4.2.2 Theory of Operation

4.2.2.1 Buffers and Level Shift for Four Scientific Signals

To scale down the 20 volt span signal (seismic, tide, free mode, temperature) to 0 to +5 volt range, an extremely good regulated reference voltage supply is needed. Meanwhile the supply must accommodate a trim element which value will be determined at the test, so that an exact four to one scaling can be obtained for the four scientific signals.

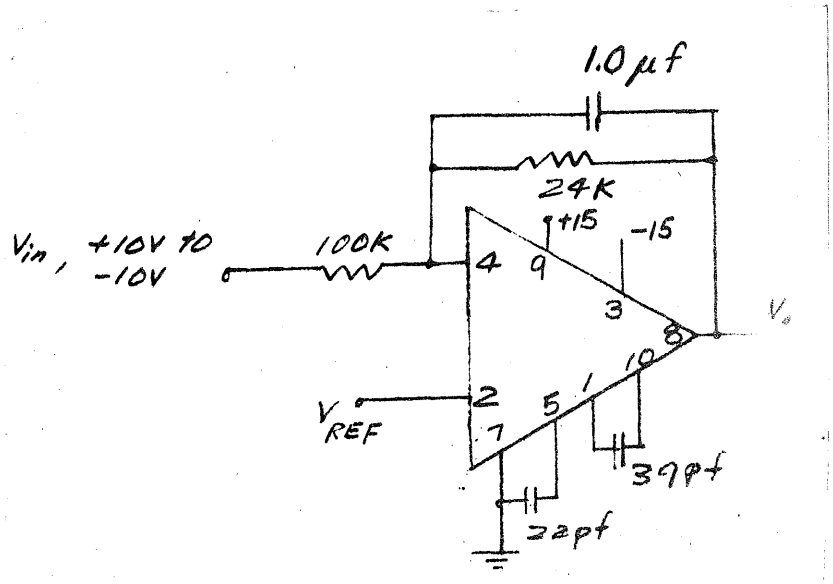


Figure 4-5 Buffer Amplifier for Four Sceientific Signals

The buffer amplifier in Fig. 4-5 is used to inversely shift the +10v to -10v range signal to a range of 0v to +5v. Normally V_{REF} is designed to satisfy the condition of the 0v input signal but with the flexibility to be trimmed and fixed at test for a desired value.

Let $V_{in} = 0V$

Normally, $\frac{V_{REF}}{100K} = \frac{V_o}{124K}$, $V_{REF} = \frac{2.5 \times 100K}{124K} = 2.02\,V$

4.2.2.2 Reference Voltage Supply

Fig. 4-6 shows the circuit of the reference voltage supply

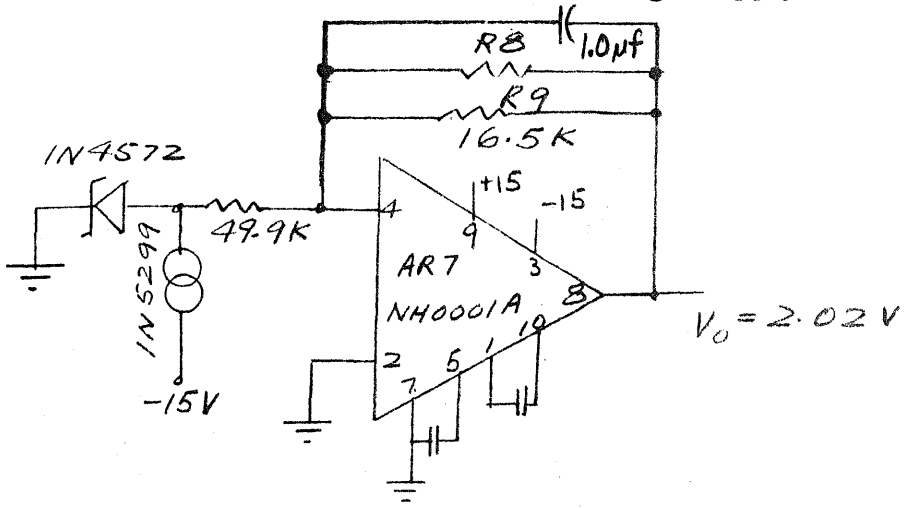


Figure 4-6 Reference Voltage Supply

From the buffer-amplifier design it was known $V_{REF} = 2.02V$. Therefore it is to design here for $V_o = 2.02\,V$.

The combination of voltage regulator IN4572 and current regulator IN5299 establishes a good regulated voltage normally 6.4 U at one end of R_{17}, then,

$$\frac{6.4\,V}{49.9K} = \frac{V_o}{R_T} \qquad R_T = R_8 \,//\, R_9$$

$$R_T = \frac{49.9K \times 2.02}{6.4} = 15.7\,K\Omega$$

R_{24} shunt with R_{25} provides the flexibility to trim V_o to be in the range of 2.09 v to 1.96v.

4.2.2.3 Buffer Amplifier for A.C. Oscillator Output

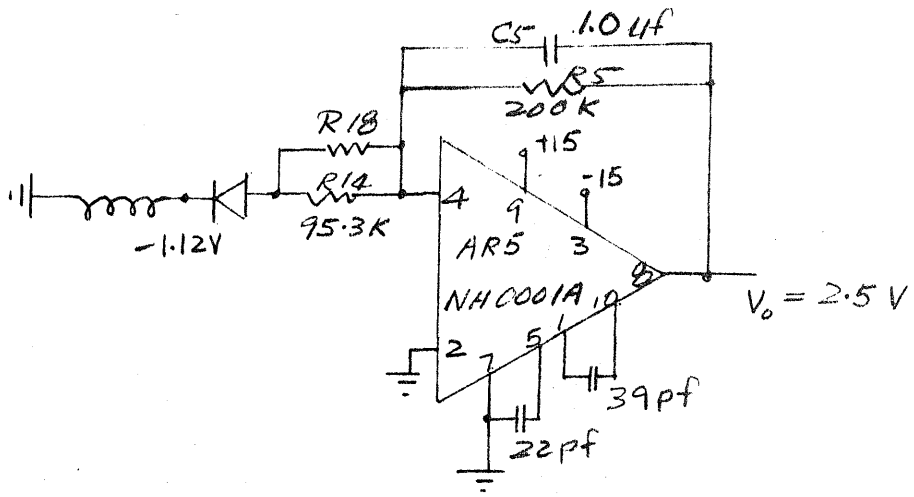


Figure 4-7 Buffer Amplifier for A.C. Oscillator Output

The peak to peak voltage for the 3.5 kc oscillator is 7v. For the half wave rectify,

$$V_{AVG} = \frac{V_p \times \frac{2}{\pi}}{2} = \frac{V_p}{\pi} = \frac{3.5}{\pi} = 1.12\,V$$

The buffer amplifier is designed to shift this average voltage to 2.5v. Due to the series connection of R_{14} to the diode, the diode forward current is only a few microamperes, the diode voltage drop is typically 0.3 volt.

Therefore $\frac{200K}{2.5V} = \frac{R_T}{0.82V}$, $R_T = R_{14} \parallel R_{18}$

$$R_T = \frac{200K \times 0.82}{2.5} = 65.8K\Omega$$

Since R_{14} = 95.3K, R_{18} is to be determined at test so that V_o can be trimmed to 2.50V.

An extremely low ripple voltage is desired for the output voltage. Assume the ripple voltage is to be less than 4 mv, the feedback capacitance is calculated:

$$G(j\omega) = \frac{\bar{v}_o}{\bar{v}_{in}} = \frac{\frac{R_5}{j\omega C_5}}{R_5 + \frac{1}{j\omega C}} \left(\frac{1}{R_{14}}\right)$$

$$|v_o| = v_{in} \frac{R_5}{R_{14}} \frac{1}{\sqrt{1^2 + (\omega R_5 C_5)^2}} = 4mv$$

$$C_5 = \frac{v_{in}}{\omega R_{14} \times 20 \times 10^{-3}} = \frac{0.82 \times 10^3}{2\pi \times 3.5 \times 10^3 \times 65.8 \times 10^3 \times 4}$$

$$= 0.15\ uf$$

4.2.2.4 Mass Position Signal

Mass position signal is ranged between -6v and 0v, it shifted to the range of 0.5v to 4.65v by a resistive divider as shown in Fig. 4-8. The output resistance of the divider is 6.9 k Ω. Following is the list of voltage conversion:

MASS POSITION SIGNAL (VOLTS	-0.179	-0.241	-0.13	-1.239	-2.253	-2.189	-3.318	-3.249	-4.26	-4.19
CONVERT. VOLT.	+4.477	+4.434	+3.7	+3.742	+3.039	+3.084	+2.301	2.349	+1.648	+1.697

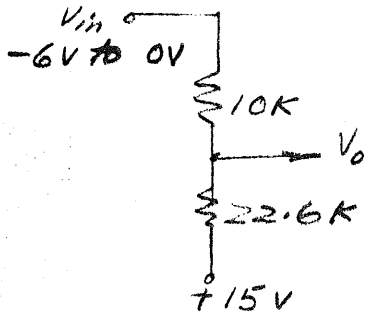


Figure 4-8 Resistive Divider for Mass Position Signal

4.2.2.5 -15v Power Supply

The -15v power supply is inversely shifted to +2.5v

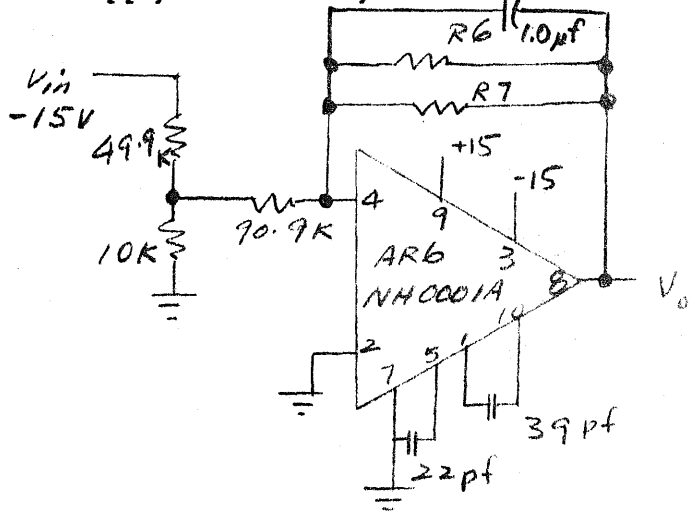
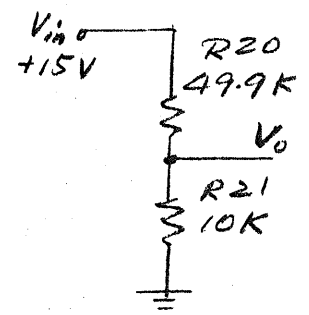


Figure 4-9 Buffer-amplifier for -15v Supply

R15 and R16 divide the -15v supply to $\frac{15 \times 10}{59.9}$ = -2.5v.. AR6 (NH0001A) provides inversion and unity gain to this voltage. The amplifier is intentionally designed at a voltage gain of 1.1 with R6 shunt the feedback resistor R7 to trim the ouuput to +2.50v.

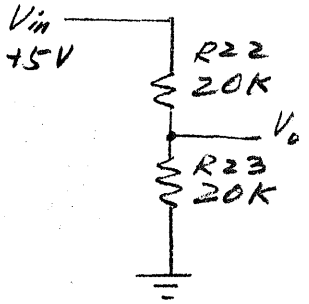
4.2.2.6 +15v and +5v Power Supplies

The +15v and +5v supply voltages are also shifted to +2.5v by a resistive divider. In Fig. 4-10 (a)



(a)

The output resistance of the divider is 8.3 k Ω .



In Fig. 4-10 (b) V_o = 2.5v
The output resistance is 10 k Ω .

Figure 4-10 Resistive Dividers for +15v and +5v supplies

SECTION 5

LSG ASSEMBLIES 2362174 & 2362175

5.1 FINE AND COARSE SCREW MOTOR CONTROL

5.1.1 General Description

The screw motor logic is located on assy 2362174. The screw Motor Drive is located on assy 2362175. The Logic is used to drive the course or the fine screw motors. It will provide control signals to the screw servo motors on command from the command decoder. On commands gross up, vernier up, gross down, or vernier down, data gate pulses are counted down by a fifteen stage binary counter. The count down system is used to control the running time of the screw servo motors. A gross command is used to operate the screw servo motor for a period of 308 seconds, while a fine command will operate the motor for a period of 2.4 seconds. An up command will slew the motor forward, and a down command will slew the motor in the reverse direction.

5.1.2 Circuit Description

Refer to Circuit Schematic No. 2362064. Data gate pulses are gated by logic element U5A to the previously mentioned fifteen stage binary count down system. Gate U5A is controlled by the motor status flip flop U 6. Refer to the block diagram, Figure 5-1.

The motor status flip flop is preset each time the module receives command signal by gate U14C. Command lines, gross up, vernier up, gross down, and vernier down are normally in the one or high state. When a low state is present on the gross up, vernier up, gross down, or vernier down input lines, a low state will be present at the preset input of U 6. A low at the preset input of U 6 will set the Q output to a high state. The Q output of U 6 is used to control gate U5A. Refer to Timing Diagram, Figure 5-3. When a high state is present at the input, control gate U5A will now pass data gate clock pulses to counters U1-U4.

Counters U1-U4 are reset by U15A. The counters will start counting data gate pulses in binary from 0 to 256 on a vernier command, or from 0 to 32,768 on a gross command.

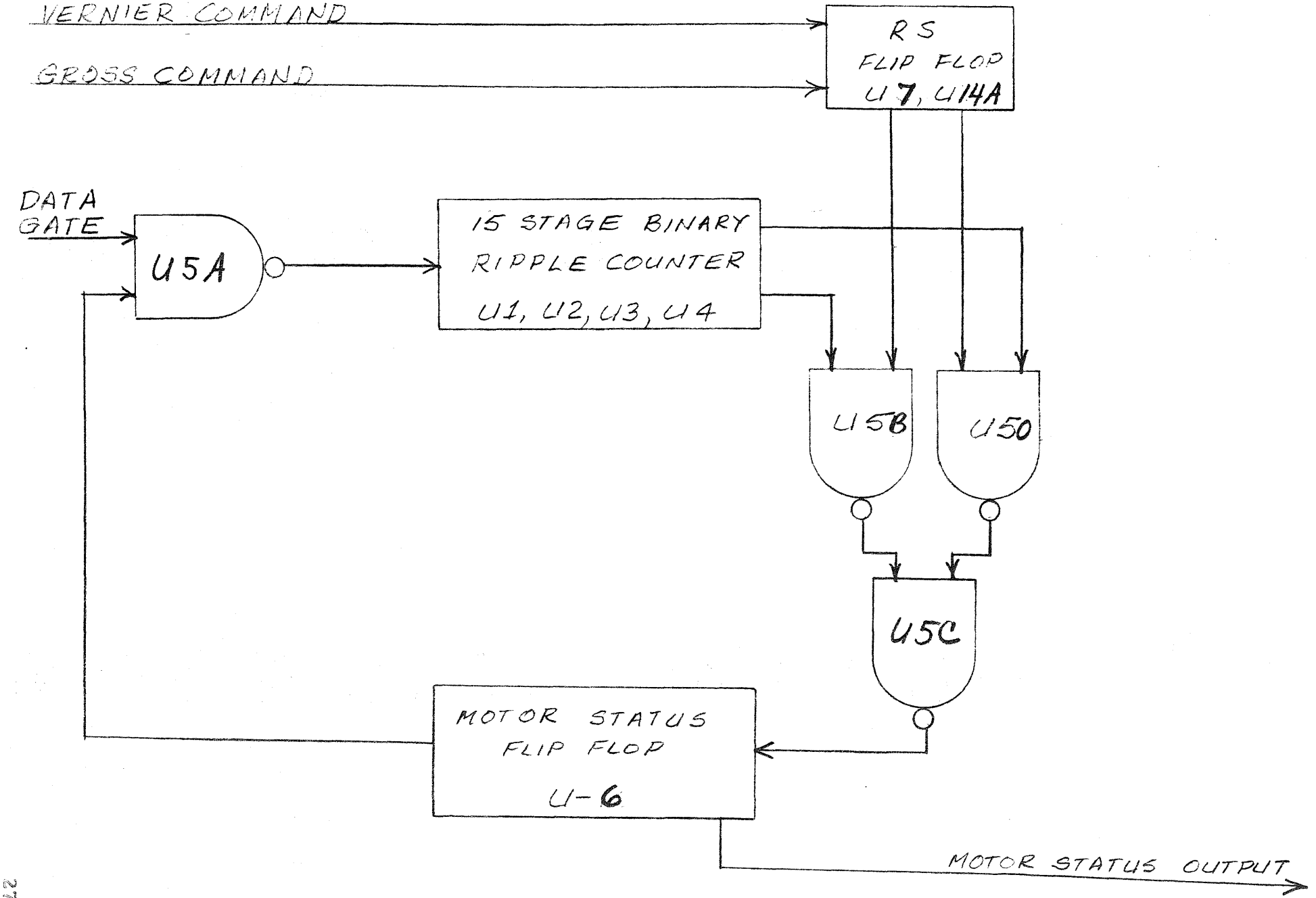


FIGURE 5-1

SCREW LOGIC CONTROL AND TIMING - BLOCK DIAGRAM

Two, three input gates, U7 and U14A were implemented to make a R-S flipflop. A low state on one of the vernier command lines will set the U76 output to a high state. Gates in U5 are implemented to reset flip-flop U6 when a binary court of 2^8 (256) or 2^{15} (32, 768) has been obtained. These gates are controlled by R-S flip flop U7 A & B and U7C & U14A. On command one side of the flip flop will be set to a high state. The gate associated with this output will go to a low state when the count down flipflop switches to a high state. When the output of the counter which was selected on command reaches overflow, gate U5-C will reset flip flop U 6. Control gate U5 A will cut off clock pulses to the counter until a new command gross up, vernier up, gross down, or vernier down is given.

Two, three input gates in U7 (A &B) were implemented to produce a R-S flip flop. When a low signal is present on one of the up command lines, output 5 on U7A will go high. The direction output of U8B will be low as a result of the high signal at the input.

A low signal on one of the down commands will set the R-S flip flop U7A pin 5 to a low state. The direction output of U8B will be high as a result of the low signal at the input. Two gates of U14 (B & C) are used to produce a low signal at the preset input of the motor status flip flop, U 6 when a low signal is present at the command on gross, or command on fine lines.

Data gate pulses, which are controlled by gate U5A are divided by two at the first stage of U1. The fifty three Hertz data gate pulses pass through a low power driver U8D to a one shot multivibrator, U9. One shot multivibrator U9 , is used to control the pulse width to the servo motors, and to clock the up/down counter U10.

Three dual input gates U8 (A, B & C) are implemented to steer counting direction commands to the UP-DOWN counter U10. This is accomplished by having the output correspond to the equations:

$$\underline{\text{UP}} \quad \text{U8B pin 8} = Q10B$$

$$\underline{\text{DOWN}} \quad \text{U8B pin 8} = \overline{Q10B}$$

but since U8B pin 8 = J10A, K10A then

$$\underline{\text{UP}} \quad J10A,\ K10A = Q10B$$

$$\underline{\text{DOWN}} \quad J10A,\ K10A = \overline{Q10B}$$

which are the equations for up/down J, K counter control. Both sequences, UP and DOWN, are shown in Table 5-1.

Decoding of counter U10 is provided by the four dual input gates of U11 (A, B, C &D). See figure 2 and 3. Table 5-1 and Figure 5-2 is a table of the decoding.

TABLE 5-1

COUNTER LOGIC DECODING

Up Sequence J10A, K10A = Q10B	Decimal	Counter Output Q10A	Q10B	Decoded Output U11- A	B	C	D	To Outpin Pin Number	Drive Transistors Switched (BD 5)
1	0	0	0	1	1	1	0	35	Q13 & Q14
2	1	0	1	0	1	1	1	34	Q15 & Q16
3	2	1	0	1	1	0	1	31	Q11 & Q12
4	3	1	1	1	0	1	1	29	Q9 & Q10
5	0	0	0	1	1	1	0	35	Q13 & Q14

etc

Dwn Sequence J10A, K10A = Q10B	Decimal	Ctr Output Q10A	Q10B	Decoded Output J11 - A	B	C	D	To Output Pin No.	Drive xtrs Switched (BD 5)
1	0	0	0	1	1	1	0	35	QB & Q14
2	3	1	1	1	0	1	1	39	Q9 & Q10
3	2	1	0	1	1	0	1	31	Q11 & Q12
4	1	0	1	0	1	1	1	34	Q15 & Q16
5	0	0	0	1	1	1	0	35	Q13 & Q14

etc

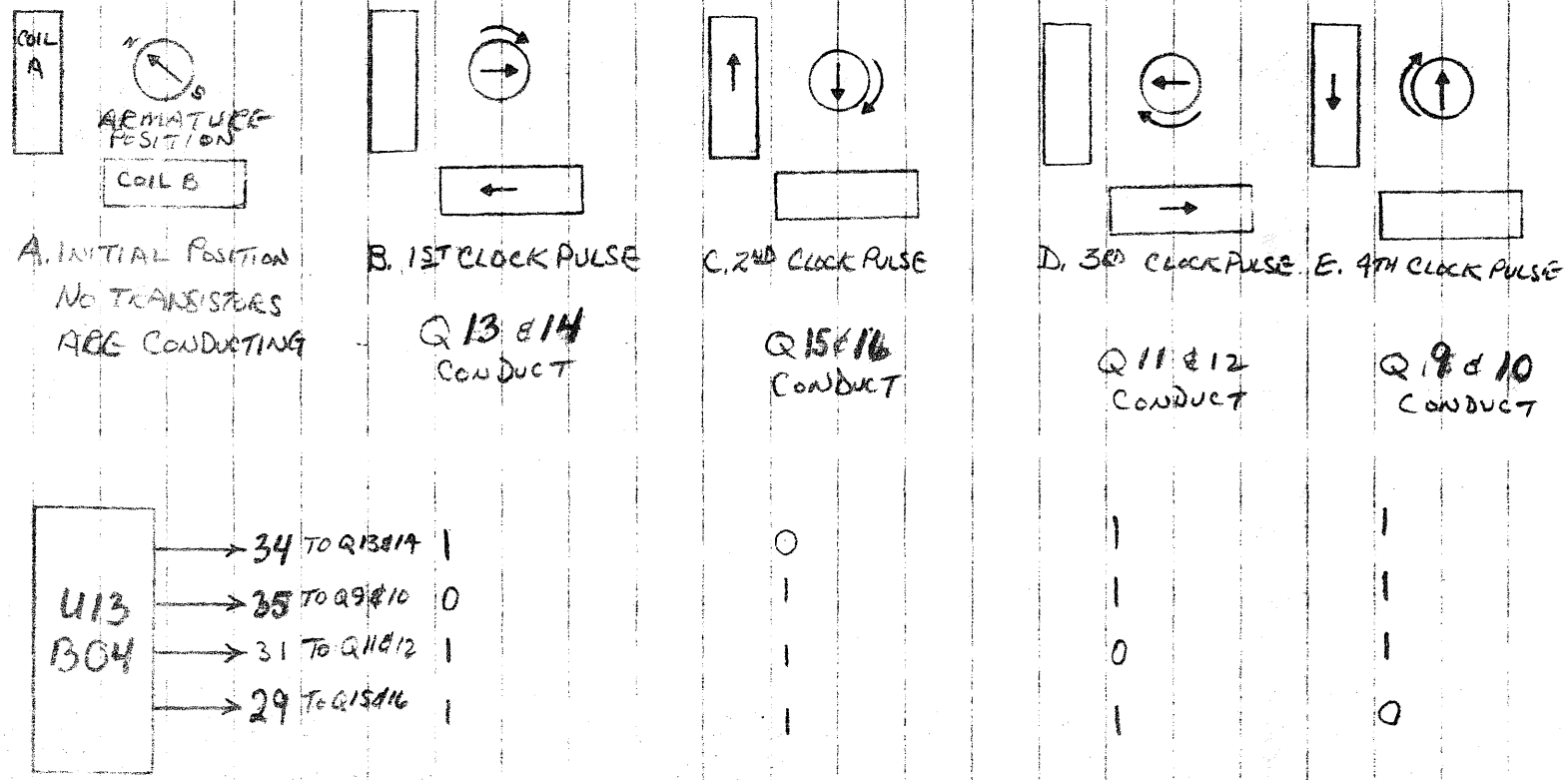
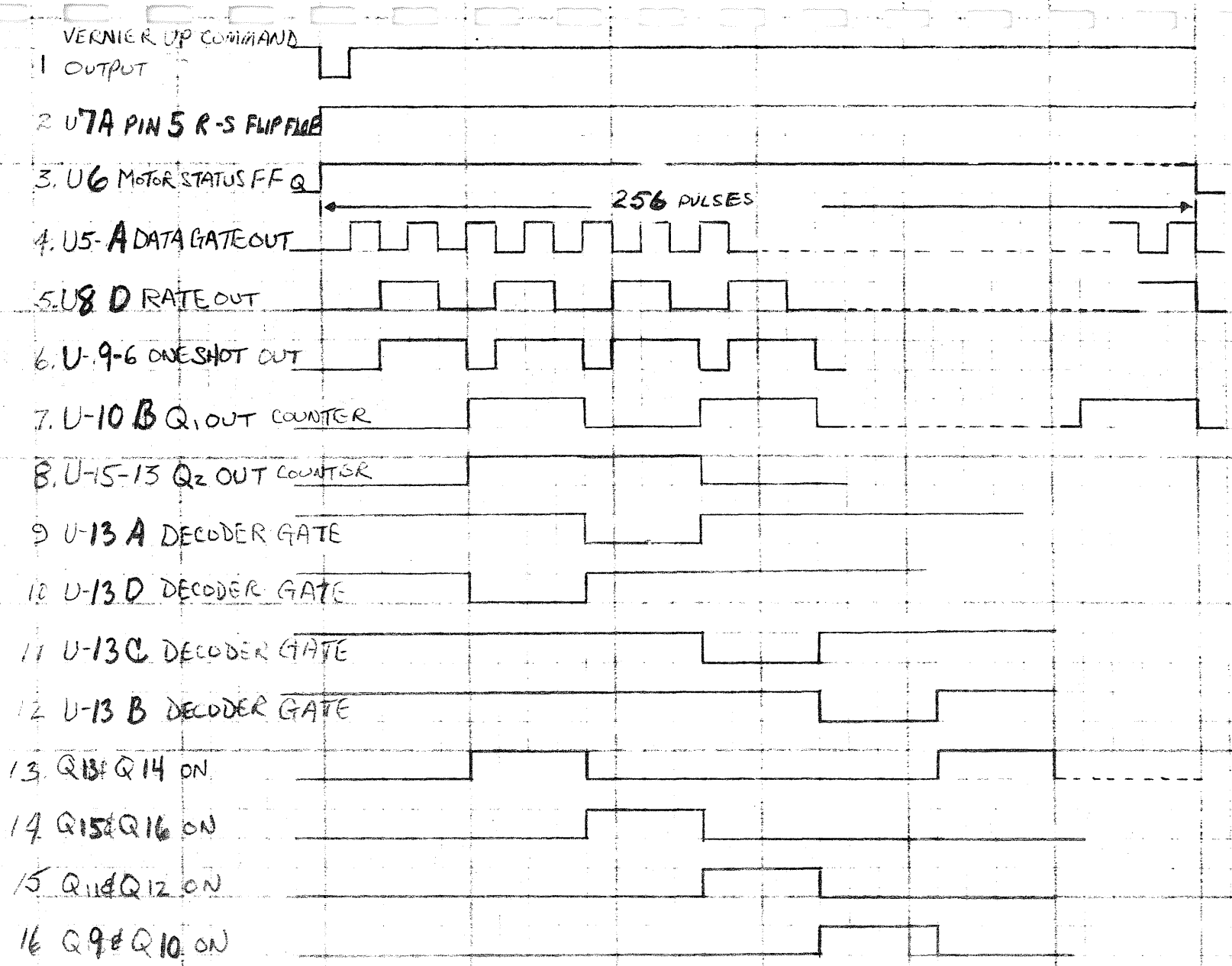


Figure 5-2 Pulse Servo Operation (Vernier-Up)



SCREW MOTOR CONTROL TIMING DIAGRAM (VERNIER-UP)
FIGURE 5-3

as the function of counter state, and the switching order of transistors Q9 - Q16, (schematic 2362320, sh2)

Transistors Q9 - 16 are used to control the screw servo motor position. Direction of the armature motion is controlled by switching the direction of current flow through the coils of the motor. Transistors Q9 - Q16 are switched in the order indicated in figure 5-2. The armature of the screw servo motor is a permanent magnet. Arrows in Figure 5-2 indicate the direction of magnetic north. As the current is switched through each coil, the magnetic flux around the coil will force the armature to align its poles in the opposite direction. Figure 5-2 A, B, C, and D, is used to illustrate the position of the armature in the screw servo motor as a function of each clock pulse from the one shot multivibrator U11.

Relay K4 is used to switch from the course to the fine screw servo motor. This switching is done on a relay command from the command decoder. Relay K5 is used to control the +15 volt power, and +5 volt power for boards 4 and 5. Relay K5 is operated on a relay command from the command decoder.

5.2 TILT CONTROL SUBSYSTEM

5.2.1 General Description

The Tilt Control subsystem is incorporated to provide command adjustment of the spatial orientation of the sensor package after placement on the moon.

The Tilt Control must provide the control and power required for the Tilt Control motor when performing Tilt adjustments after command. Because of system power limitations, the Tilt Control must minimize power consumption between commands. This is accomplished by providing power on/off switching capability.

The Tilt Control Subsystem is comprised of two sections - the logic portion (Assy 2362174) for determining the timing and step control for the Pulsed Step Servo motor and the analog drive circuit (Assy 2362175) to deliver the pulse power required by the motor.

Additionally, since there are two motors required to perform the leveling operation (north-south and east-west directions,) a relay selection circuit is included at the output of the analog drive circuit to select the desired motor.

5.2.2 Circuit Description

References

1. Schematics
   a. (Logic) #2362064
   b. Drive #2362320

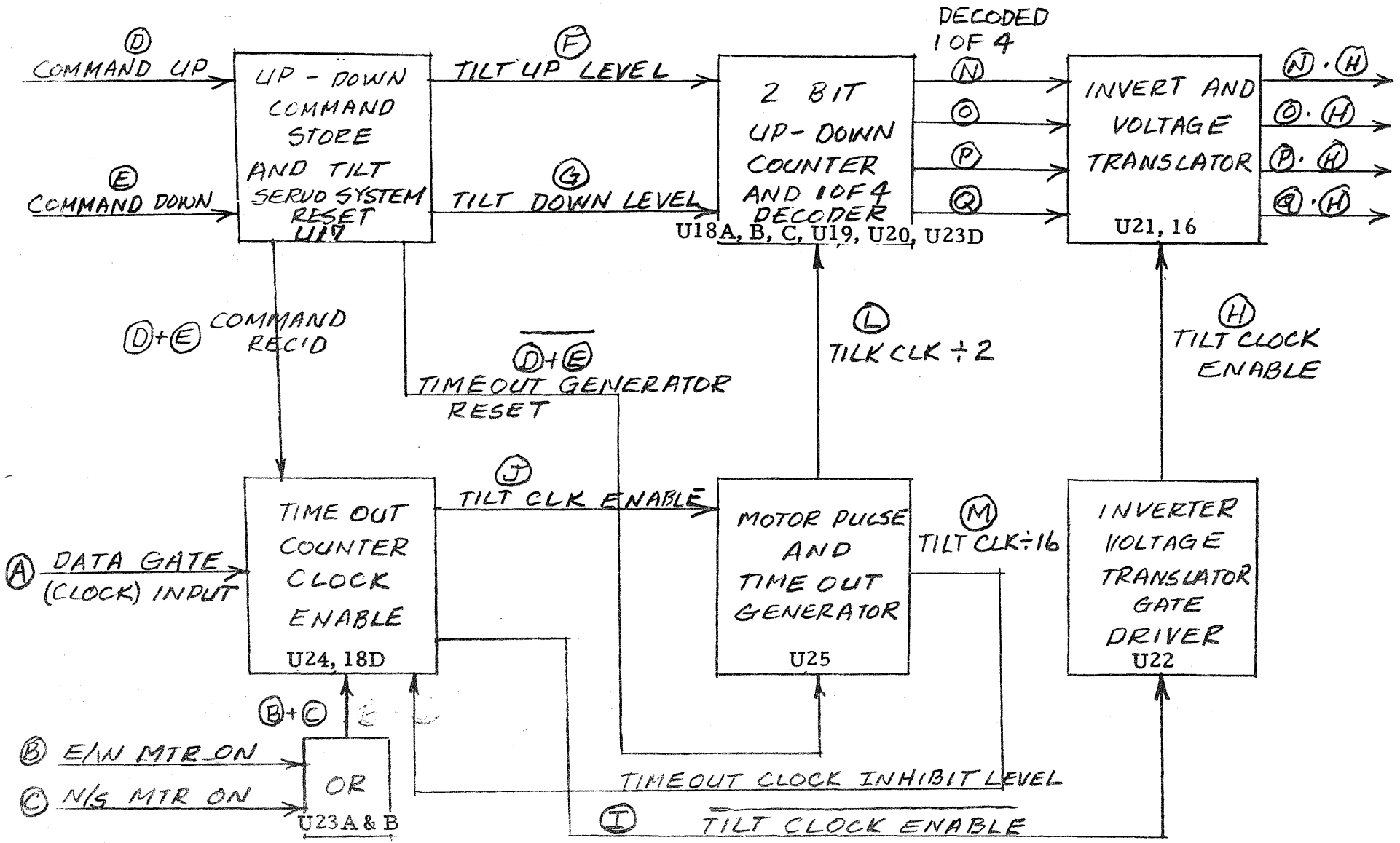
2. Functional Diagram
   a. Block Diagram - Fig. 5-4
   b. Analog Drive - Fig. 5-6

3. Logic Timing Diagram - Fig 5-5

Circuit description for the Tilt Control Subsystem will be accomplished into two parts: one part the logic timing and control will be described first, followed by the analog drive circuit contained on board 5.

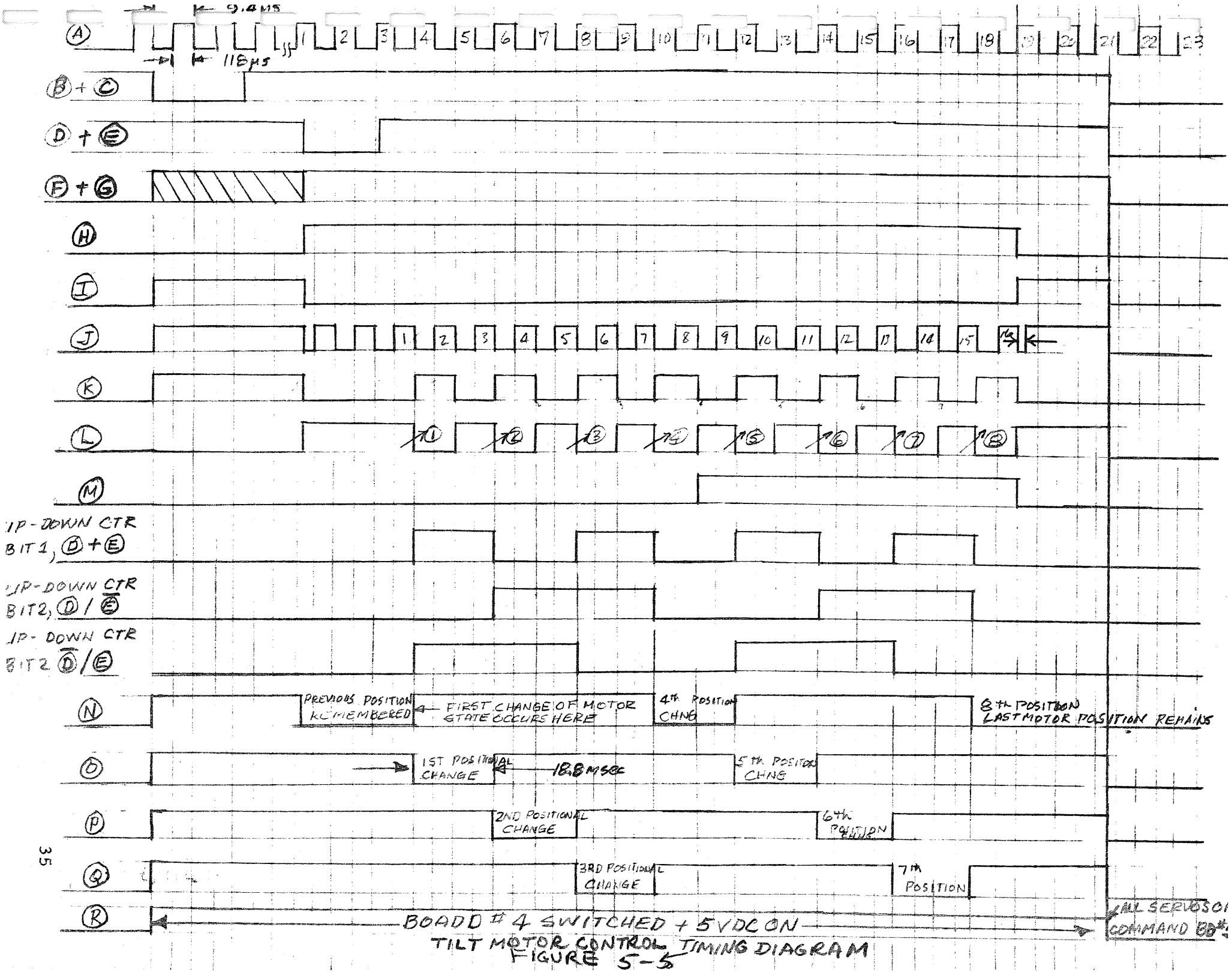
5.2.3 Logic Timing and Control

Refer to figures 5-4, 5-6 and schematic 2362316. The timing rate for the logic portion of the Tilt Control Subsystem is obtained from the "data gate" (A) input supplied by the digital buffer circuit. As illustrated by the timing diagram, this signal is present continuously, at the input, pin 23. The logic is powerized (+5VDC) coincidentally with either the "E/W or N/S logic motor on" signals. These signals are "or'd" together with the resulting output (B) + (C) presetting the timeout counter clock enable (U-24), thus immediately inhibiting the "data gate", input gate [(U-180) & timing diagram, (J)]. This condition remains until the leading edge of either the "Up-Command" or "Down-Command," which are also or'd. together [(D) + (E) in U-17 C&D] providing a timeout counter clock enable to the data gate input gate, thus allowing the "data gate" to clock the input of the "Motor pulse and timeout generator". This generator, however, will not react to this input clock until the trailing edge of (D) + (E) passes, since this signal acts as a counter inhibit until the data gate enable has been accomplished. The "Motor Pulse and Timeout Generator" consists of a 16 bit MSI ripple counter U-25, where the first stage halves the input clock frequency and forms a square wave pulse train of eight pulses which will drive the "2-Bit Up-Down Counter (U-19) in the commanded direction. After the 16th input clock pulse, the "Motor Pulse and Timeout Generator" emits a down-going edge (M) from its last stage, which is fed back to the clock input of the timeout counter clock enable, inhibiting

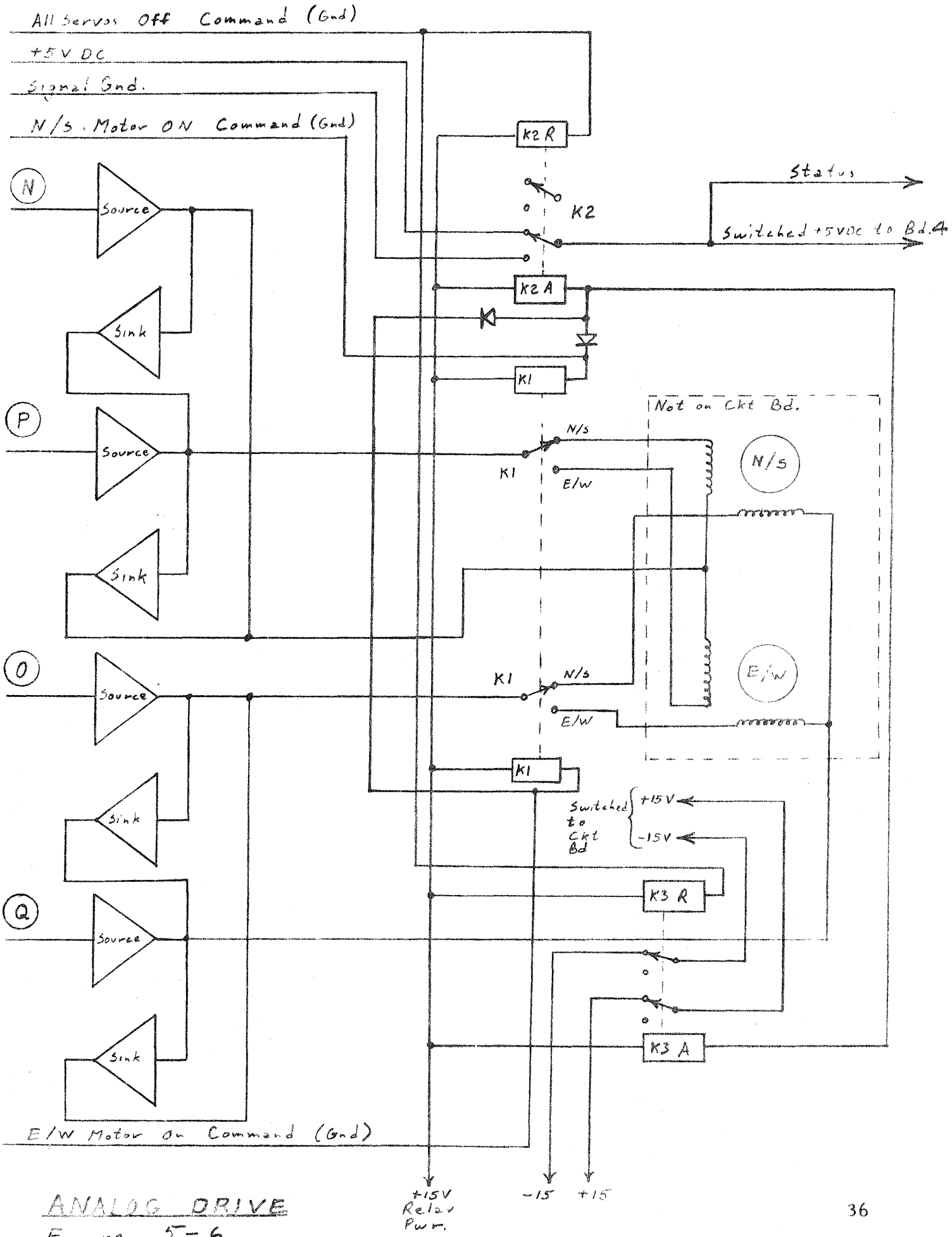


BLOCK DIAGRAM - TILT CONTROL SUBSYSTEM

FIGURE 5-4



TILT MOTOR CONTROL TIMING DIAGRAM
FIGURE 5-5



ANALOG DRIVE

Figure 5-6

the data clock input until the next "Command-Up" or "Command Down" pulse is received. The 2-Bit Up-Down counter derives the direction of count from the "Up-Down command store "R-S flip flop, comprised of two gates in U18 A, B and C, which produces a signal at F or G depending on the commanded direction. For the UP SEQUENCE J_{ul9b}, K_{ul9b} = Q19A and for the DOWN SEQUENCE J_{ul9b}, K_{ul9b} = Q19A. Either of these levels are steered to the 2-Bit Up-Down counter, via U18D, to provide the proper JK inputs to U19B, thus establishing a counting direction (Note: both the Up and Down counts are shown in the timing diagram, but the decoding is for the Up-Count only.) The sequential states of the Up-Down counter are then decoded by a 1 of 4 decoder establishing a 1 of 4 hot output lines to the "Invert and Voltage Translators" (N) (O) (P) (Q). The Voltage Translators (U-16), utilize the logic O to +5VDC, to sink current from a +15VDC source and are enabled only during the 16 count by a signal (I). This signal enables the output during the same time window used for the clock enable. U-22, is required to buffer low level logic (U-24) to high level logic (U-16). It is worthy to note that once the leveling process is completed, +5VDC Logic power (Logic) is switched "off" by a relay. (Ref: Analog Drive Block Diagram, Figure 5-5).

5.2.4 Analog Drive CKT

Refer to Figure 5-6. Prior to receiving digitally processed time control pulses from the "Tilt Logic Timing and Control" section #1 either the "N/S motor on" or the "E/W motor on" will select the desired motor to be commanded. These inputs are grounding relay control signals and are time coincident with the signals of the same nomenclature (B) + (C) that start the logic. Additionally, they are non-coincident with each other and the application of either will switch +5VDC to board #4 via the diode "or" gate to the +5VDC relay (K2) and simultaneously apply ±15 VDC power to board 5 via Relay K3.

After the power is applied to both circuit boards, the analog drive circuit must wait for either the "up" or "down" sequence of pulses (current sink commands) to be sent from the Logic Timing and Contrd Section to the analog drive circuit. Each input line receives two ground sink pulses in the sequence (N), (P), (O), (Q), in the same time relationship as illustrated on the digital timing diagram (Fig 5-5). Each pulse causes current to flow from the source amplifier to the motor through the preselected relay path. The source amplifier also biases the sink amplifier "on" thus allowing it to sink the motor coil current supplied by the source.

5.2.5 Power Requirements

As described previously all power (+5VDC, ±15VDC is command switched via relays K2 and K3 to both the digital and analog sections of the Tilt Control Subsystems. Power is turned off when the "All Servos off" relay command is applied to relays K2 and K3.

5.3 CAGE MOTOR CONTROL

5.3.1 General Description

The need for the Cage Control circuit stems from the LGE System requirement for immobile arrestment of the Sensor package during transportation including the flight to the moon. The Cage Control circuit is capable of delivering the required current to the Cage Control Motor during either command cage or command uncage mode of operation as desired. Due to power considerations, the control circuitry is also required to shut down automatically (without command) after the motor has accomplished the caging or uncaging operation.

5.3.2 Circuit Description

References

1. Schematic #2362320 Page 3
2. Block Diagram Fig. 5-7
3. Analog Timing Diagram Fig. 5-8

A 20 millesecond ground signal applied to either Command Cage Pin 69) or Command Uncage (Pin 63) from the Command Decoder activates the Cage Control circuit. When either of these non-coincident signals appear, the DPDT relay K6, is set to the Cage or Uncage position on the leading edge of that input command. K6 determines the direction of rotation; hence whether the motor cages or uncages the sensor package.

Simultaneously, either ground input command is steered through CR32 or CR34, to provide a negative 20 millesecond pulse to a RC differentiator circuit, comprised of C13 and R51. The resulting positive spike (see timing diagram formed by the RC differentiator is steered through CR35 to the gate of Q17, a MOS FET, operated as an enhancement mode (Type C) high input impedence buffer. The positive spike

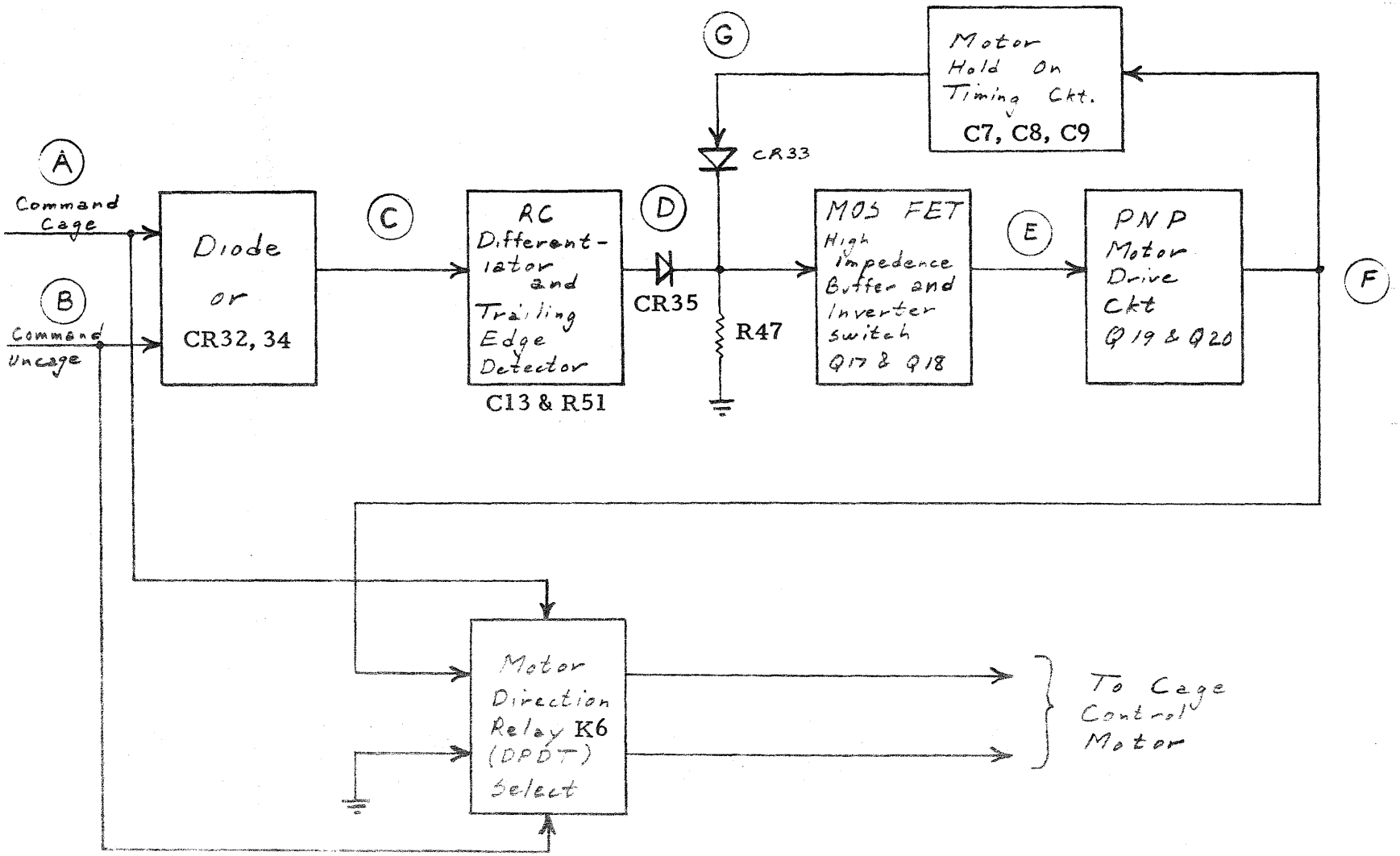


FIGURE 5-7

CAGE CONTROL CIRCUIT - BLOCK DIAGRAM

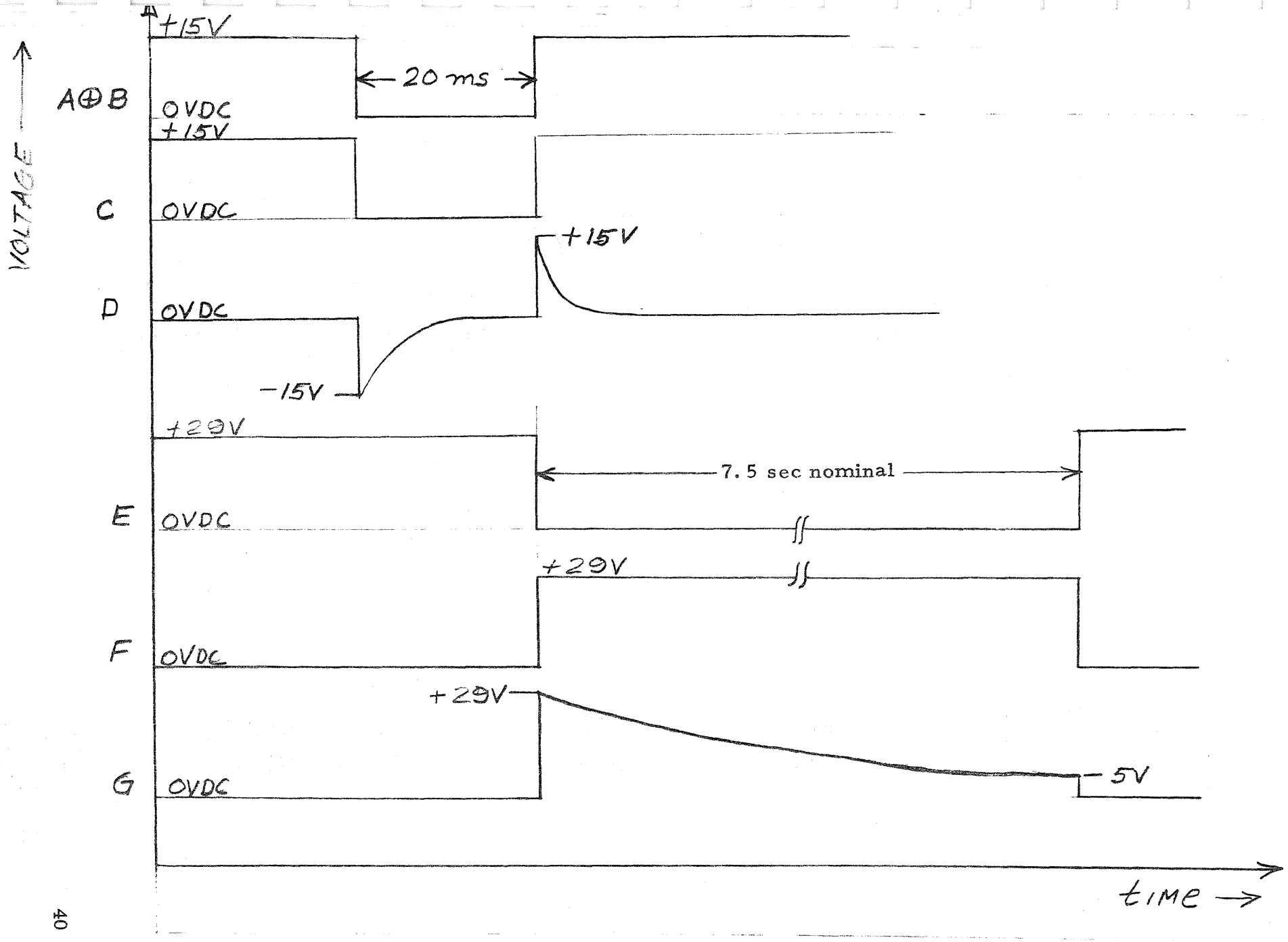


FIGURE 5-8
CAGE CONTROL CIRCUIT- TIMING DIAGRAM

causes sufficient current to flow in the source of Q17 to allow Q18 to saturate, forcing current drivers Q19 and Q20 into conduction. Q19 and Q20 provide the required current needed by the Cage Control Motor via the motor direction select relay (K6) for a period of time (approx \7.5 sec - see timing diagram), established by the regenerative voltage feedback path through C7/C8/C9 to the gate of Q17. This voltage, V_{R47} (see timing diagram), causes Q17 to continue conducting, thus holding Q18 saturated and Q19 and Q20 conducting current to the motor. The droop is caused by C7/C8/C9 charging and its rate is determined by the R43 and C_7/C8 time constant. When the drooping feedback voltage falls below the MOS FET threshold voltage, Q17 turns off causing Q18, Q19 and Q20 to also turn off, thus stopping the cage control motor.

The motor current "on" time can be computed using the relationship:

$$T_{on} \tilde{=} 2.3\ R_{47} \cdot (C_7 // C_8 // C9)$$

Since the present mechanical design requires the motor to operate for at least 5 seconds to insure either the complete cage or uncage operation. R47 and C_7//C8/C9 have been choosen to provide $To_n \tilde{=} 7.5$ seconds thereby insuring complete operation by a factor of better than 50%This is necessitated by component nominal value variations with age, temperature etc.

POWER REQUIREMENTS

As per the preceeding circuit description, this functions has been designed to consume power only when the cage control motor actually performs a commanded function. Additionally, the +29VDC voltage input is switched "on" prior to either command cage or uncage by virtue of the Instrument Heater +29V Power ON~OFF relay. The +29V power to the cage control is available when the Instr Htr Power relay is in the OFF position.

SECTION 6

LSG ASSEMBLY 2362176

6.1 MASS CHANGE SERVO CONTROL

6.1.1 General Description

The Mass Change Control Subsystem is required from a system viewpoint in order to select the proper mass quantity required to perform lunar gravity measurements. Five Mass Change States are selectable:

1 All Masses Caged (Reset)
2. All Masses On
3 1st Lunar Mass off
4 2nd Lunar Mass off
5 Main Lunar Mass off (Earth Mass only)

The first State is provided to safeguard the mass changing system during transportation and the fifth state is used primarily on earth for calibration purposes. The remaining states consist of mass combinations that can be selected to roughly place the sensor within its dynamic range during Lunar gravity measurements.

The Mass Change Control Subsystem must provide a method for deciphering and correlating and the mass condition desired by input command. It must also provide a circuit to drive the motor which performs the mass change operation. Finally, it must provide motor position feedback to halt the motor drive when the motor has established the desired mass change state.

Additionally, a special requirement exists due to the mechanical design of the Mass change coupling system. The Mass Change Motor drives a slotted gear which in turn hits a pin that drives the mass change system. To preclude mechanical linkage, the pin must not rest against the gear slot after the proper mass has been selected. This is accomplished by adding a substate to each of the Mass Change States. These states, occuring on the next increment

command sequentially after the selection of Mass Change States, cause the motor to reverse direction for approximately 1/2 the arc length of the slot, thus leaving the pin free of mechanical contact with the gear slot.

6.1.2 Circuit Description

6.1.2.1 References

6.1.2.1.1 SCHEMATIC # 2362069
6.1.2.1.2 BLOCK DIAGRAM - Figure #6-1

6.1.2.2 Power Section

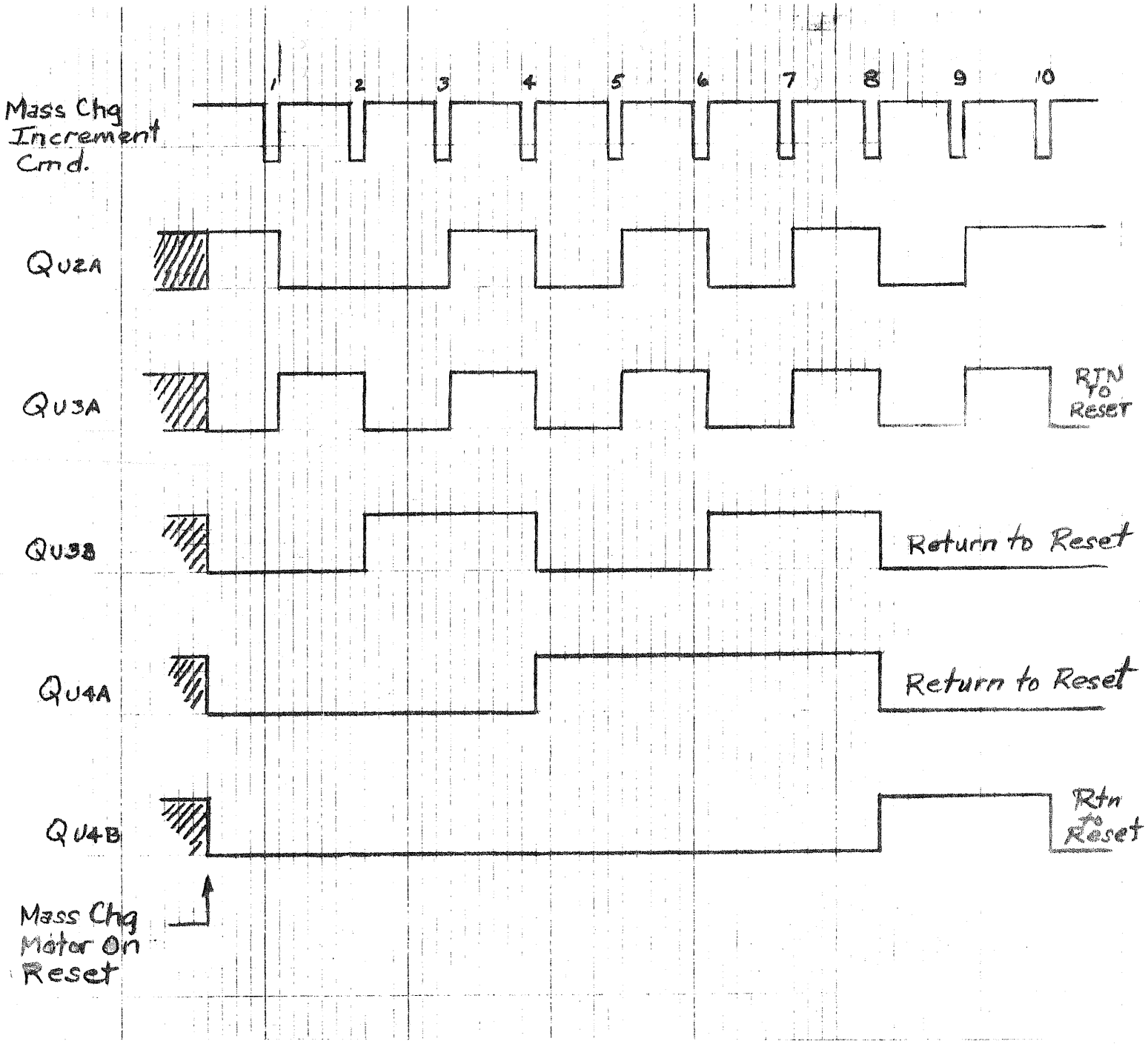
The Mass Change Control Subsystem is actuated by the "MASS CHANGE MTR ON CMD" relay grounding signal which toggles relay K2 to the "ON" state applying +15VDC and +29VDC to the Mass Change circuitry. +29 VDC will only be available to K2 if the SLAVE HEATER CONTROL circuitry is off, otherwise pin 8 of K2 will be open. +5 VDC for the logic circuits and the D to A current switches is developed from the +15 VDC by zener reference diode VRIO nd resistor R47. This voltage is also used to provide the descrete status indicator for the Mass Change Control provided to the DGTL LINE BFR/RCVR COMMAND (BOARD NO2) on pin 28. When the Mass Change Control circuits are on, +5 VDC is present on pin #28, otherwise pin 28 is at ground. -15 VDC is also required for the Operational Amplifiers but because of the very low power consumption of this voltage, -15 VDC is not switched.

6.1.2.3 Logic Section

A modified modulo 5, 3 Flip-Flop counter, is used to define the basic mass change statis described in section 6.1.1 and to provide the half slot width motor reversal logic required to leave the Mass Change Drive pin free of mechanical contact with the driving gear slot. After the "MASS CHANGE MTR LOGIC RESET" has preset the counter (U2, U3, U4) successive logic commands clock the circuit via a gate (U1C) to a state corresponding to one of five Mass Change States. Each basic mass change state has an associated motor reversal substate following it on the next command. The modulo 5 counter consists of U3B, U4A, U4B and gates U1A and U1B. This is a standard technique J, K 5-up count circuit where the clock is obtained from a device by 2 Flip-Flop U3A. U3A is required to provide the intermediate motor reversal definition is one direction when proceeding from state one through five and is just the opposite when reseting or proceeding from state five to state one, a decoding Flip Flop U2A is provided whose control inputs are defined as:

$$J_{(u2A)} = Q_{(u3A)} \qquad K_{(u2A)} = \overline{Q}_{(u4B)}$$

and whose output Q2A, illustrated below, provides the correct sequence of motor reversal after each mass change basic state.



Mass Change Timing Diagram

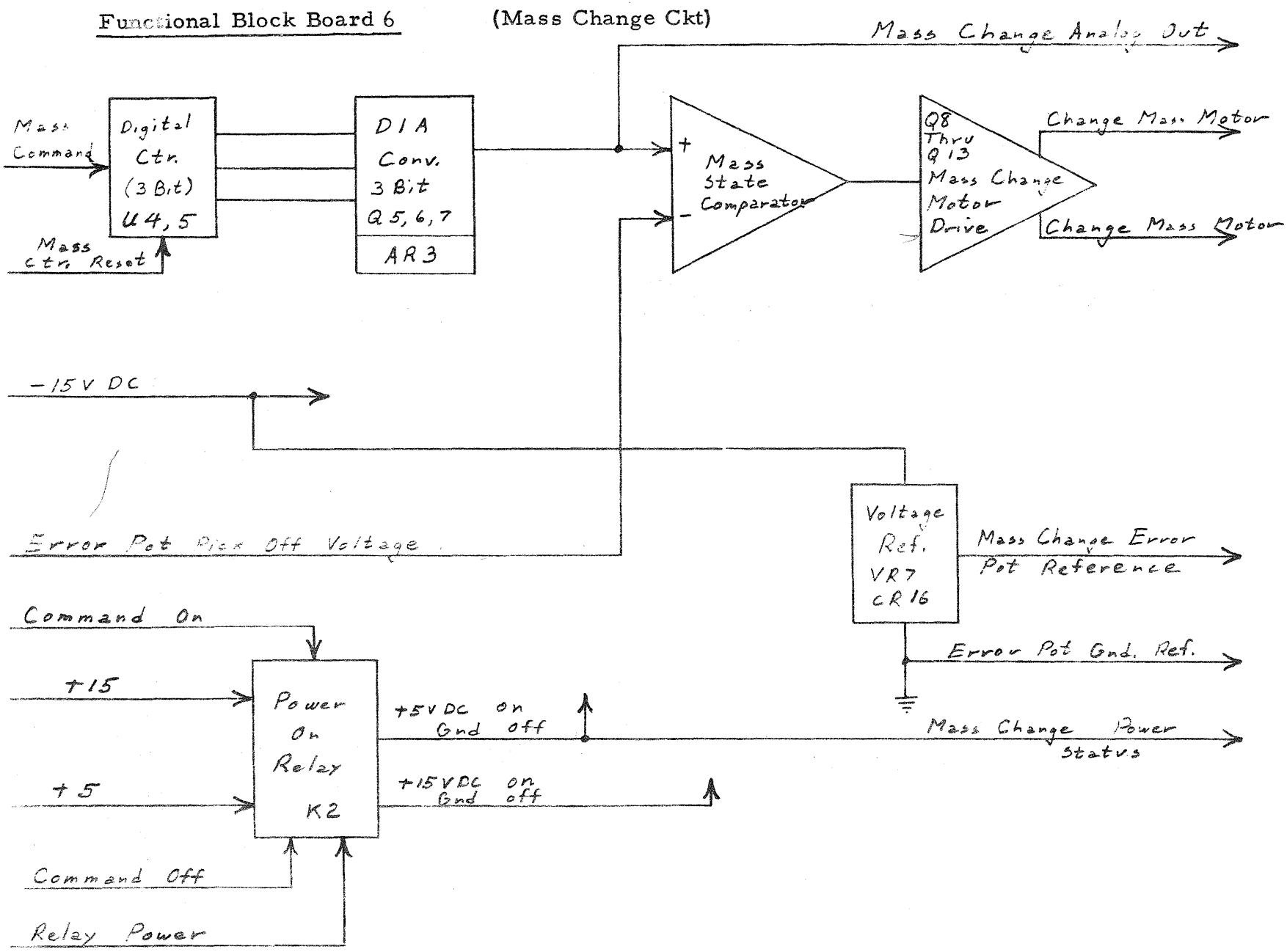


Figure 6-1 Functional Block Diagram-Mass Change Servo Control

6.1.2.4 Digital to Analog Current Switches and Voltage Transfer

Digital to analog conversion is accomplished by transistor switches Q1 through Q4 by decoding any digital counter state selected by the influent increment command and producing a total current ($IT = \Sigma Ic\ x + IR10$) to pin 4 of AR1 which is proportional to the particular state held by the digital counter. This is possible since each collector resistor is selected to produce a binary weighted current to represent the flip-flop state that is saturating that transistor. Therefore the relationship exists such that:

$$I_C{}^2 = 2\ IC_4 = 4\ I_{C_3}$$

where

$$I_{CX} = \frac{5.1\ (\text{zoner reference voltage})}{RC\ x\ (\text{collector resistor})}$$

which results in the lunary quantity

$$Qu3B\ Qu4A\ Qu4B = 2^2 2^1 2^0 = I_{C2} + I_{C4} + I_{C3}$$

being decoded as a single analog voltage quantity at the output of the inverted mode Operational amplifier AR3.

This can be accomplished by using the two operational amplifier principles that:

1. The input impedence of AR3 is extremely high in relation to all other impedences seen at input pin 4 of AR3; therefore:

$$I_{R15} = -\sum_{x=1}^{4} Icx + IR10 = Ic2 + Ic4 + Ic =$$

and 2. The voltage at pin 4 is approximately equal to the voltage at pin 2, so that pin 4 is considered a "vertual ground", therefore:

$$Eo\ (AR3) \cong E_{R15}$$

but

$$E_{R15} = I_{R15}\ R15$$

so

$$Eo(AR3) = -\sum_{x=2}^{4} I_{CX}\ R15$$

The last expression defines the analog voltage equivalent to the selected binary state.

Since the motor position potentiometer will have its lower (reset) state at a position other than zero, an idle or reset current has to be supplied to give Eo (AR3) a DC bias voltage equivalent to the lowest state at reset. This current is supplied to pin 4 of AR3 through resistor R10, thus modifying analog voltage equation to:

$$Eo(AR3) = - \left(\sum_{x=2}^{4} ICX + IR10\right) R15$$

Finally, the motor reversal (backup) voltage to compensate for the pin/slot mechanical problem is supplied through transistor Q1 as a current to be summed with IR10 when proceeding from reset to state 2 or to be deleted when transfering from any other state.

Therefore the analog voltage equivalent to a backed off motor position voltage takes on the absolute value determined by:

$$Eo(AR3) = - \left(\sum_{x=2}^{4} ICX + IC1 + IR10\right) R15$$

Once this voltage has been established, differential comparator AR4 will seek a null between pin 2 and pin 4 where pin 2 is a wiper arm potentiometer voltage proportional to motor position. AR4 then switches the motor current drive circuit "on" until the motor positions the mechanically linked potentiometer so that a null is developed between pins 2 and 4 at the input of AR4. The motor then enters a limit cycle until a new analog voltage is established by a new input command to the input ripple counter.

CR16, VR7 and R57 establish a reference voltage for the motor potentiometer and is sent to the pot via pin 63.

6.1.2.5 Motor Driver

The control circuit for supplying +29 VDC to the Mass Change Motor consist of toggle relay K3 and its driving transistors Q5 and Q6.

Differential Comparator AR4 switches between +5V to -5V depending on the direction it wishes the motor to drive. If pin 2 is more positive than pin 4, pin 8 will be at +5V and Q5 will be on, placing +29 volts from K2 on pin 3 of K3 and Alsep ground on pin 8 of K3. Should pin 4 of AR4 be more positive than pin 2, pin 8 of AR4 will be at -5V, turning Q6, on. This causes the motor to drive in the opposite direction by placing +29 VDC on pin 8 of K3 and Alsep ground on pin 3.

6.2 INSTRUMENT HOUSING HEATER CONTROL

6.2.1 General Description

The heater box and sensor assembly, is contained within a hermetically sealed instrument housing filled with dry nitrogen in order to maintain a stable environment. The instrument housing has heaters mounted on its outer surface and its temperature is controlled with a $\pm 0.05°C$ range at a temperature approximately 0.5°C lower than the heater box temperature. This stable environment is required for the heater box temperature to be controlled within $\pm .001°C$ of its set temperature. The heaters are a combination of four bifilar wound blanket heaters and four RER 65 resistors. The resistors are mounted on the four outside webs and the blanket heaters are mounted on the outside surfaces between the webs.

6.2.2 Circuit Description

A simplified schematic of the controller is shown in figure 6-2. To establish the 0.5°C differential from the heater box temperature, a differential thermistor bridge is utilized with one thermistor (RT1) on the heater box for a reference and one (RT2) on the instrument housing for a control sensor. The bridge resistors are selected to balance the bridge with the instrument housing at a temperature 0.5°C lower than the heater box. R4, R5 & the thermistors are initially selected so that an additional resistance, R6, is required to balance the bridge with a 0.5°C offset. This resistance is then calculated using the following formula.

$$R_6 = \frac{RT2\ R4 - RT1\ R5}{RT1}$$

Values for RT1 & RT2 are selected from the individual thermistor calibration data by recording a value of RT1 at the sensor spring inversion temperature and a value of RT2 at a 0.5°C lower temperature than that for RT1. The supply voltage for this bridge is a 6.4 volt temperature compensated zener driven with a field effect current regulator diode. This gives an extremely stable bridge voltage regardless of temperature or power supply fluctuations.

A National Semiconductor NH 0001A operational amplifier (AR1) is used to detect bridge imbalance and its output is an analog voltage signal which is limited at approximately ± 5 volts, DC. The amplifier gain will produce an approximately $\pm$ 0.3 volt signal for a $\pm 50\Omega$ change in RT2 resistance. This corresponds to approximately $\pm$ .125°C change in temperature when the thermistor used is YSI 44032 operating at 50C. A seven volt peak to peak square wave at approximately 15 khz is received from the power converter and is integrated to produce a symmetrical triangular

wave of 0.6 volt amplitude. Refer to figure 6-3. A second NH0001A (AR2) is used as a differential comparator between the analog output signal from the bridge amplifier and the triangular wave form. This second amplifier then becomes a pulse width modulator as long as the bridge amplifier output is in the $\pm$ .3 volt range. When the output is above +.3 volts, the pulse width modulator output will stay negative and when the output is below -.3 volts, the output will stay positive. The triangular wave and the $\pm$ .3 volts are referenced to +10 volts. Three high beta transistors follow the pulse modulation Op-amp to assure saturated switching of the heater current. The pulse load is decoupled from the ALSEP supply line by the addition of a 30 μ fd. capacitor to the heater return with a 15 ohm resistance in series. Since part of the heater power is dissipated in this resistance, four 60 Ω RER 65 resistors are paralleled and mounted, one on each instrument housing web, to distribute the heat.

To maintain the required isolation between the ALSEP signal return and the ALSEP power return, it was necessary to build +10 volt and +20 volt regulator circuits into the heater controller to provide regulated voltages referenced to the ALSEP heater return. The regulated voltages available from the LSG power converter are referenced to ALSEP signal return. National Semiconductor LM105 monolithic voltage regulators are used for the regulating elements. These voltage regulators are designed so that by selecting two resistors for an external voltage divider, output voltages of from 4.5 volts to 40 volts can be regulated to within $\pm$ 0.1%. These voltage regulators are supplied from the ALSEP Heater Voltage line.

A relay (K1) is included in the circuit to switch the instrument housing heater on & off. When the heater is switched off the two operational amplifiers are still on, but the pulse width modulator is held off by heater voltage being switched to its negative input through a high resistance by K1. In order to eliminate a high inrush charging current current for the 30 μ fd. de-coupling capacitor whenever the instrument housing heater is switched on by relay K1, the capacitor is held in a charged state through a diode and resistance from the off contact of K1. This is required by current transient constraints on the ALSEP Voltage Outputs.

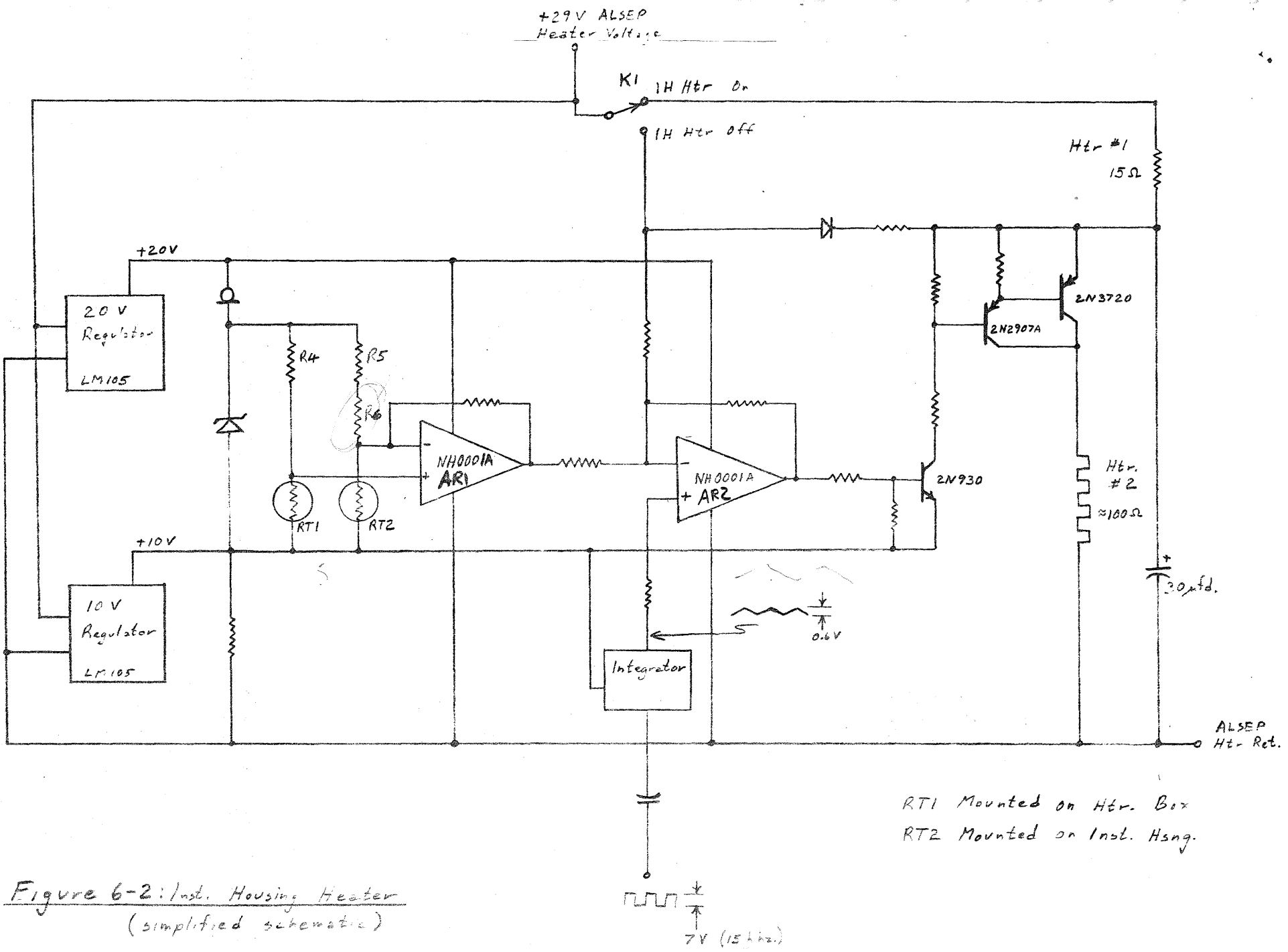


Figure 6-2: Inst. Housing Heater
(simplified schematic)

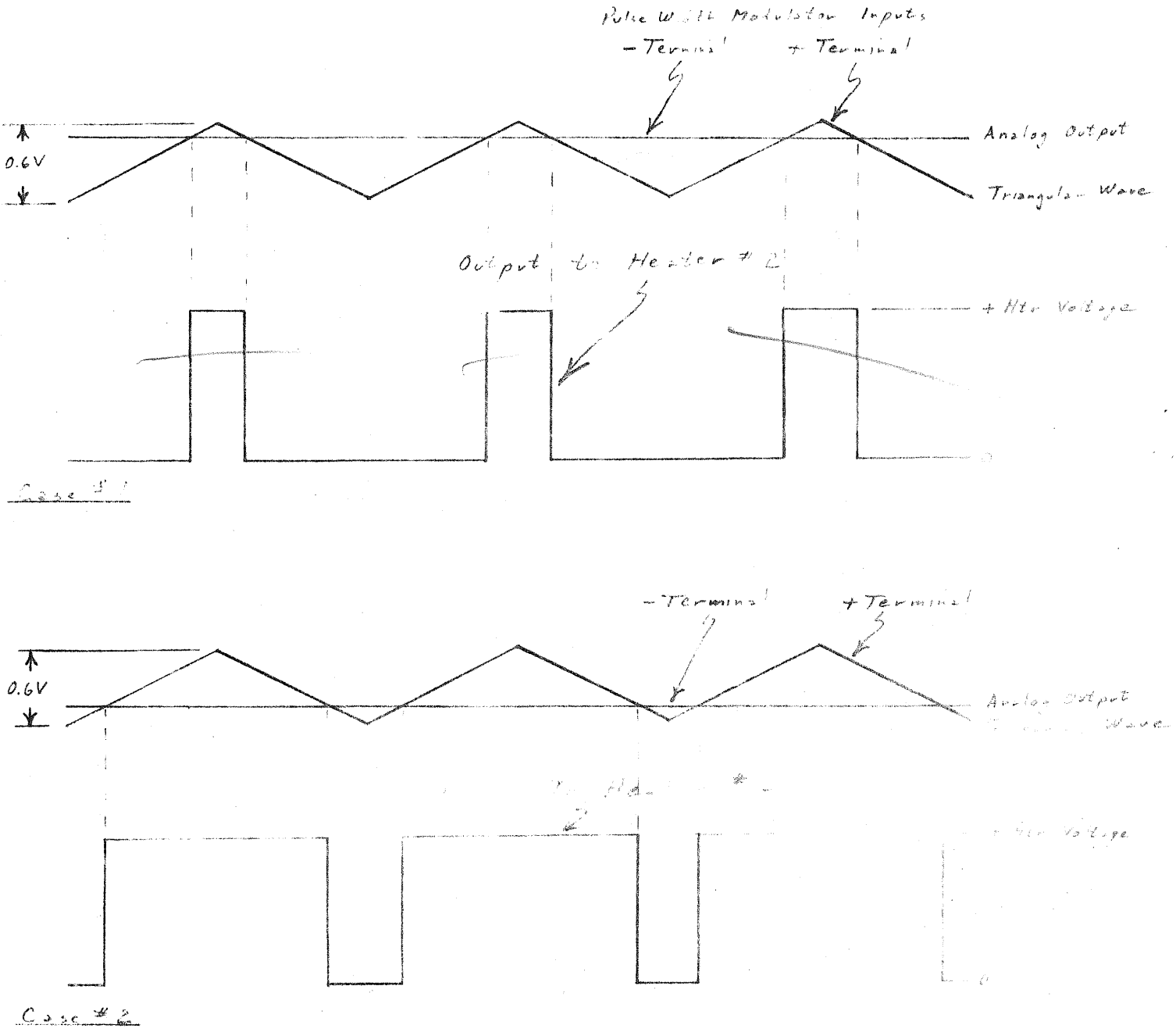


Figure 6-3 Pulse Width Modulator Operation

SECTION 7

LSG ASSEMBLY 2362177 & 2362187

7.1 FREE MODES FILTER

7.1.1 General Description

Lunar gravity has high frequency components which are caused by one of the normal modes of oscillations of the moon. There, signals are of sufficiently low frequency (. 0008 Hz to . 1 Hz) that they are detected by the sensor but are of very low magnitude are therefore further amplified and filtered by the free-modes filter.

7.1.2 Circuit Description

The Free Modes Filter receives its signal input from the tidal signal output line of the integrator, amplifies signal frequency components between . 000835 Hz and 0.1 Hz corresponding to the free modes vibrations of the lunar mass by a factor of 250, and delivers its output to the analog signal multiplexer and an analog line buffer.

Referring to Figure 7-1, AR4 together with C14 through C17, R19, R21 comprise an active 2-pole Butterworth high-pass filter with a low corner frequency of . 000835 Hz (1 cycle/20 minutes). R20, R23 set the in-band gain to 250. C13 provides an upper rolloff frequency of 0.1 Hz (6 cycles/minute), R24 through R27 provide an output offset trim capability and are adjusted during assembly to adjust the output d-c offset voltage of the amplifier below the quantization level on the output data line.

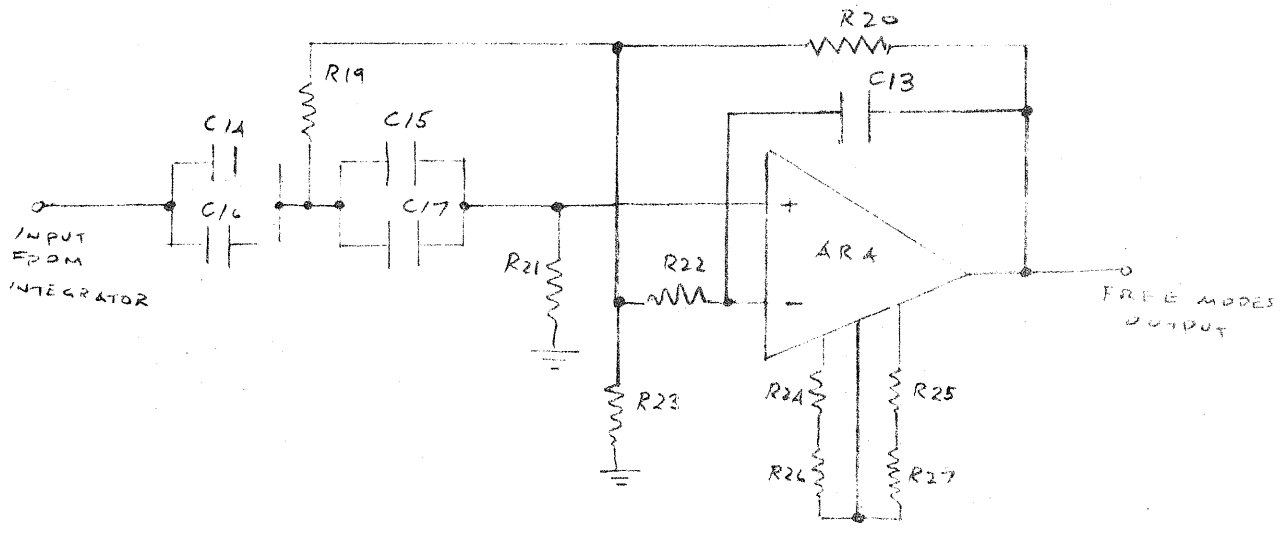


Figure 7-1 Free Modes Filter

7.2 SEISMIC FILTER

7.2.1 General Description

The Low Data Rate Seismic Filter receives the signal output of the demodulator R-C filter, amplifies seismic signal frequency components between .05 Hz and 1.65 Hz by a factor of 2000, and delivers its output to the analog signal multiplexer and an analog line buffer. The band-pass characteristic is achieved by a cascade connection of a low-pass active filter having an upper cutoff frequency of 1.65 Hz followed by a high-pass active filter with a low corner frequency of .05 Hz. The output stage includes a d-c output offset trim capability and additional band-limiting upper roll-off to minimize any broadband noise contribution of the second stage.

A parallel low gain low-pass signal path is provided for monitoring beam position during initial system setup during operation in the screw servo mode.

The High Data Rate Seismic Filter is the same as the Low Data Rate Seismic Filter except:

a. It has a high frequency corner at 16.5 Hz instead of 1.65 Hz.

b. The High pass active filter is a 4 pole instead of a 2 pole Butterworth active filter.

7.2.2 Circuit Description: Low Data Rate Seismic Filter

The Seismic Filter design is detailed on schematic 2362113 AR1 together with R4, R5, C5, C6 comprises an active 2-pole Butterworth low-pass filter with an upper cut-off frequency of 1.65 Hz. R6, R7 set the in-band gain of the first stage to 20.

AR2 together with C8, C9, R2, R8 comprise an active 2-pole Butterworth high-pass filter with a lower corner frequency of .05 Hz. R9, R10 set the in-band gain of the second stage to 100.

The resulting overall filter characteristic of the two stages in cascade is in-band gain of 2000 with lower and upper cut-off frequencies of .05 Hz and 1.65 Hz respectively.

R11 through R14 in AR2 provide an output offset trim capability and are adjusted during assembly to keep the output d-c offset voltage below the quantization level on the output data line. C10 provides an upper roll-off frequency on the second stage to limit the upper noise bandwidth and

minimize the effect of second stage noise. This also provides additional rejection to any carrier frequency residue in the output of the demodulator R-C filter.

AR3 provides the low gain seismic output. This direct coupled monitor of the demodulator output is utilized during initial setup operation in the screw servo mode to monitor beam position during open loop operation. Relay K1 transfers the seismic output line between the high gain seismic amplifier and the low gain seismic amplifier upon execution of the corresponding commands. Another contact of K1 provides a logic "1" indication of seismic status when the seismic high gain amplifier is in use.

7.2.3 Circuit Description: High Data Rate Seismic Filter

The Seismic Filter High Data Rate design is detailed on schematic 2362475. The 4-pole Butterworth active filters are obtained with AR3 for the first stage and AR4 for the second stage. The filter for the first stage is determined by C14, C15, R16, R17 while C11, C17, R18 and R19 determines the response of the 2nd stage. The inband gain of the low pass filter combination is determined by R20 and R28 and is set at 20. Note that the two stages individually are not 2-pole Butterworth filters but operate as a whole as a 4-pole Butterworth filter.

AR5 together with C12, C13, R22 and R23 constitute the high pass 2-pole Butterworth filter with R30, C20 providing a high frequency roll-off to filter high frequency signal that might appear in this last stage. The gain of 100 is obtained with R30 and R29. R24, R25, R31 and R32 provide the offset trimming for the last stage.

AR6 provides the low gain seismic output as in the low data rate. The switching from the high gain to the low gain seismic filter is done with relay K2.

7.3 INTEGRATOR

7.3.1 General Description

The integrator provides the capability for sensor to operate close to null position. It enable the system to measure low frequency signals (tide and free-modes) with minimum error.

7.3.2 Circuit Description

Refer to schematic for High Data Rate for the following discussion. The integrator receives its signal from the demod output. The integrator time constant is determined by R34 and C19 to provide 50 sec. period. Capacitor C19 is chosen such that it has a high leakage resistance so that the circuit operates as an integrator to as low a frequency as possible. The offset trimming is provided by R13 and R14.

On integrate normal mode of operation the output of the integrator is feed to the Free Modes filter. On integrate short mode capacitor C19 is shorted by means of the latching relay K1 through R26. Also the Free Modes input is transferred to the output of the seismic low gain amplifier.

SECTION 8

LSG ASSEMBLY 2362178

8.1 POST AMPLIFIER

8.1.1 General Description

The Post Amplifier receives the carrier signal output of the pre-amplifier and delivers the amplified carrier signal to the phase sensitive demodulator in the electrostatic loop. The gain of the post amplifier is digitally controlled by command to provide control of the electrostatic loop gain. A limiting circuit is incorporated to prevent phase shift effects due to amplifier overloading by large signals such as would occur in open loop operation. The frequency compensation of the amplifier minimizes the phase shift in the amplifier at carrier frequency.

8.1.2 Circuit Description

The amplifier is a non-inverting circuit form to facilitate digital control of the gain. The close loop gain is determined by the ratio of R31 to the equivalent parallel resistance of R35 through R38. Refer to schematic 2362332, Sheet 2. The gain is controlled by using the 4 bit binary code stored in a command-actuated 4 bit counter to control the state of four FET switches which connect in sixteen different combinations of the four resistors R35 through R38.

U4 and U5 are dual J-K flip flops connected to form a 4 bit binary counter. Successive executions of the Post Amplifier Gain Increment Command applied through inverter U3 advances the binary number stored in the counter. The Q sides of the counter flip flops drive the input lines of U1 and U2, a pair of dual FET switches with integral drivers. A high state in the Q input opens the associated FET switch removing the ground return of the associated gain control resistor, reducing the post amplifier gain. Conversely, a low state in the $\overline{Q}$ input closes the FET switch returning the lower end of the gain control resistor to ground, increasing the post amplifier gain. Execution of the Post Amplifier Gain Reset Command causes a high state in all counter $\overline{Q}$ states, open all FET switches, removes all

gain control resistors R35 through R38, and sets the Post Amplifier to unity gain. Fifteen successive executions of the Post Amplifier Gain Increment Command increases the gain in the sequence 6, 12, 18, ..., 84, 90 numeric gain. Execution of the sixteenth gain increment command also resets the counter and establishes unity gain.

VR1 through VR4 and CR11 and CR12 comprise a limiting circuit which sets the output limit level of the post amplifier to $\pm$10.2 volts. The limiting network prevents the operational amplifier from swinging to the limits of the power supply voltages to avoid phase shift effects in the leading and trailing edges of the amplified signal if saturation were not prevented.

8.2 OSCILLATOR, DEMODULATOR, AND BRIDGE

8.2.1 General Description

The Oscillator, Demod, and Bridge circuit are parts of a carrier amplifier system which can detect small changes in the relative position of the gravimeter plates. The pre-amp and post-amp precede this circuit. The oscillator generates the 3.3 KC carrier signal which is applied as a sine wave to the bridge transformer, and as a square wave to the demod input. The bridge transformer supplies equal AC signals of opposite phase to the two fixed gravimeter plates. The center, movable gravimeter plate picks up an AC voltage which is dependant in phase and amplitude on its position between the plates. This voltage is amplified in the pre-amp and post-amp and applied to one terminal of the demodulator circuit. The other terminal of the demodulator circuit is fed from a square wave derived from the 3.3 KC oscillator. The DC output of the demodulator is proportional in amplitude to the input AC signal and of polarity dependent on its phase.

8.2.2 Circuit Description

The reader is referred to schematic 2362332, Sheet 1. The oscillator proper is composed of operational amplifier AR4, a positive feed back network which peaks at the frequency of oscillation; and a resistive divider negative feed back which is adjusted for the required AC output level. (Known as the Wien Bridge Circuit). The frequency dependent positive feedback networks at the noninverting input of the op-amp consist of: (a) parallel RC network (R27 & C18) to ground for attenuation of high frequency signals, and (b) a series RC network (R30 & C21), to the output of the amplifier for attenuation of low frequency signals. At the frequency of oscillation the divider has a gain of approximately 1/3.

At the inverting amplifier input a 47K resistor (R21) goes to the output, and a 22K and 4.7K resistor (R24 and R29 respectively) are in series from the input to ground. The combined feedback network adjusts the circuit for approximate equal positive and negative feedback. An FET in parallel with the 4.7K acts as a variable resistor so that the two feedbacks can be made exactly equal.

The resistance of the FET (Q3, 2N4857) is controlled by a feedback loop. The oscillator output is fed back through resistors R_1 and R_3 to the inverting input of OP amp AR1. Resistor R5 acts as an attenuator to control the level at the input and CR2 keeps the signal from going negative. Amplifier AR1 acts as a positive peak comparator. When the sine wave peak at the negative input of the amplifier exceeds the reference DC value on the positive input of the amplifier (as generated by constant current diode CR1, zener VR5, and divider resistors R10 and R12,) a sharp negative spike is generated at the amplifier output. This spike charges capacitor C-15 through diode CR9. The resultant exponentially decaying signal is integrated by R23 and C-20. The resultant minus DC level turns the control FET off. Thus, initially, positive feedback in the oscillator is greater than negative feedback, the μ level of oscillation builds up until control amplifier AR1 conducts and biases the FET off to the point where equilibrium is maintained.

If one assumes that a one volt peak to peak signal is necessary at each gravimeter plate then the signal at the primary is equal to 1 x 14.15 (step down ratio of transformer). The peak value is one half of this or 7.07 volts. If we assume that R-12 is infinite then the reference voltage is equal to the zener voltage (6.4 volts). At the moment of comparison the negative inputs of AR1 must be slightly greater than 6.4 volts.

If we neglect the current through R2 then the top of R1 is

$$\frac{(4.7 + 22.1 + 221)(6.4)}{221} = 7.15$$

The resistors were adjusted empirically for correct output. The disagreement between theory and practice is probably in the error of the transformer ratio.

Operational amplifier AR-2 is used to square the oscillator sine wave for use in driving the reference input to the demod. It functions simply as an overdriven amplifier. The capacitors and resistors in the input circuit can be used to shift phase as necessary to meet system requirements.

The demodulator proper is fed by the 3.3 KC sine signal from the post-amp at the primary of T1. The square wave reference is inserted at the primary of T-2. Both T1 and T2 have push-pull secondary windings. The two 2N4857 FET's are turned on during alternate half cycles of the 3.3 KC wave and thus act as phase sensitive switches. Self bias is developed for the switches by resistors R-13, R19, R14 and capacitor C-12. When the Gate ends of the square wave driving transformers go positive, the Gate conducts. R13 and R19 limit the Gate current and clip the Gate drive wave form. The current drawn by the Gates also flows through R14. The resultant voltage is smoothed by capacitor C12.

Since the square wave secondary winding system is connected only to the demod output, the voltages on it move up and down with the demod output. All square wave currents flow through the FET gate and source only and do not affect the signal. Current flows through R13 and R19 for 1/2 cycle only but flows through R14 for the full cycle. The current is equal to the peak voltage of 1/2 the secondary winding divided by the total resistance (33 K + 330 K = 363 K). Since the winding ratios for the T-37 are 1:1:1 and the square wave primary is swinging approximately 27 volts PP then the 1/2 cycle gate current is $I = \frac{13.5}{363 \times 103} = .037$ MA and the bias voltage developed across the 330 K resistor is $\frac{330}{363} \times 13.5 =$ 12.7 volts.

The demod output is filtered by 10 K resistor R-15 and UF capacitor C-19. The maximum DC voltage out of the demodulator is $\frac{2}{50}$ (V peak) or 7 volts. The filtered demod output signal is fed to the seismic amplifier. It also drives integrator AR 3.[1] The integrator time constant is 10 megohms R22 and 10 microfarads C13 or 100 seconds. The 1402-02 OP amp as used here was chosen for low current drift and high output swing. Provision is made for shorting the integrator and simultaneously connecting the points fed by it to ground. This function is performed by the latching relay K8 when commanded by the command decoder.

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[1] EM-1 configuration only

The "bridge" circuit consists of transformer T-2, resistors R8 and R9 and various trimming and by-passing components. The function of the bridge circuit is to apply 3.3 KC 1 VPP signals of equal amplitudes to the gravimeter plates. A DC voltage differential between the plates is provided by a precision external biasing source presently specified at 4.05 volts currently. A battery is used to provide the DC bias. However, a zener reference may be incorporated in subsequent models. Resistors R8 and R9 serve to connect the DC center point of the floating bridge and supply to the tidal signal so that one of the gravimeter plates is more positive than the tidal signal by 1/2 the DC source and the other plate is more negative by 1/2 the DC source. C2 and C5 serve to bypass the source voltage so that differential mode AC signals are attenuated. Capacitor C3 bypasses common mode bridge signals to ground. The value of this capacitor cannot be increased indefinitely because it, together with resistors R8 and R9 in parallel, form a time constant in series with the system loop.

Latching relay K1 connects the precision bias voltage into the bridge circuit or connects the bottom legs of the bridge to ground. This feature is useful for eliminating battery drain during storage and is necessary because the battery must be removed during system centering adjustments.

SECTION 9

LSG ASSEMBLY 2362333

9.1 ANALOG TO DIGITAL CONVERTER

9.1.1 General Description

The outputs from Filter, Integrator, Temperature sensor and Demodulator are analog signals. Analog to digital converter is essential if these scientific signals are to be processed, transmitted and displayed as digital data.

The voltage comparison technique is the basis for the A-D converter. The successive approximation method is used due to its relatively speedy and accurate conversion. A digital to analog converter is used to provide a variable reference voltage which follows the input analog voltage.

In the successive approximation method, the conversion process consists of starting with the most significant bit (MSB) and successively trying a logic '0' in each bit of a D-A converter. Logic 0 is the state needed to activate the analog gate for each digital bit (refer to Figure 9-1). The output of the D-A converter V_{REF} is compared to the input analog voltage V_{AI} as each bit is tried. If the D-A output voltage is greater than V_{AI} the '0' state is removed from that bit and the next MSB is tried. When V_{AI} is greater than the D-A output voltage, the '0' state remains with that bit and next bit is tried. This process repeats until the least significant bit has been tried. The digital bits in the D-A converter are bit states which drive analog gates, and the complement of the bits state is the digital conversion of the input analog voltage.

9.1.2 Circuit Description

The functional block diagram of A-D converter is shown in Figure 9-1.

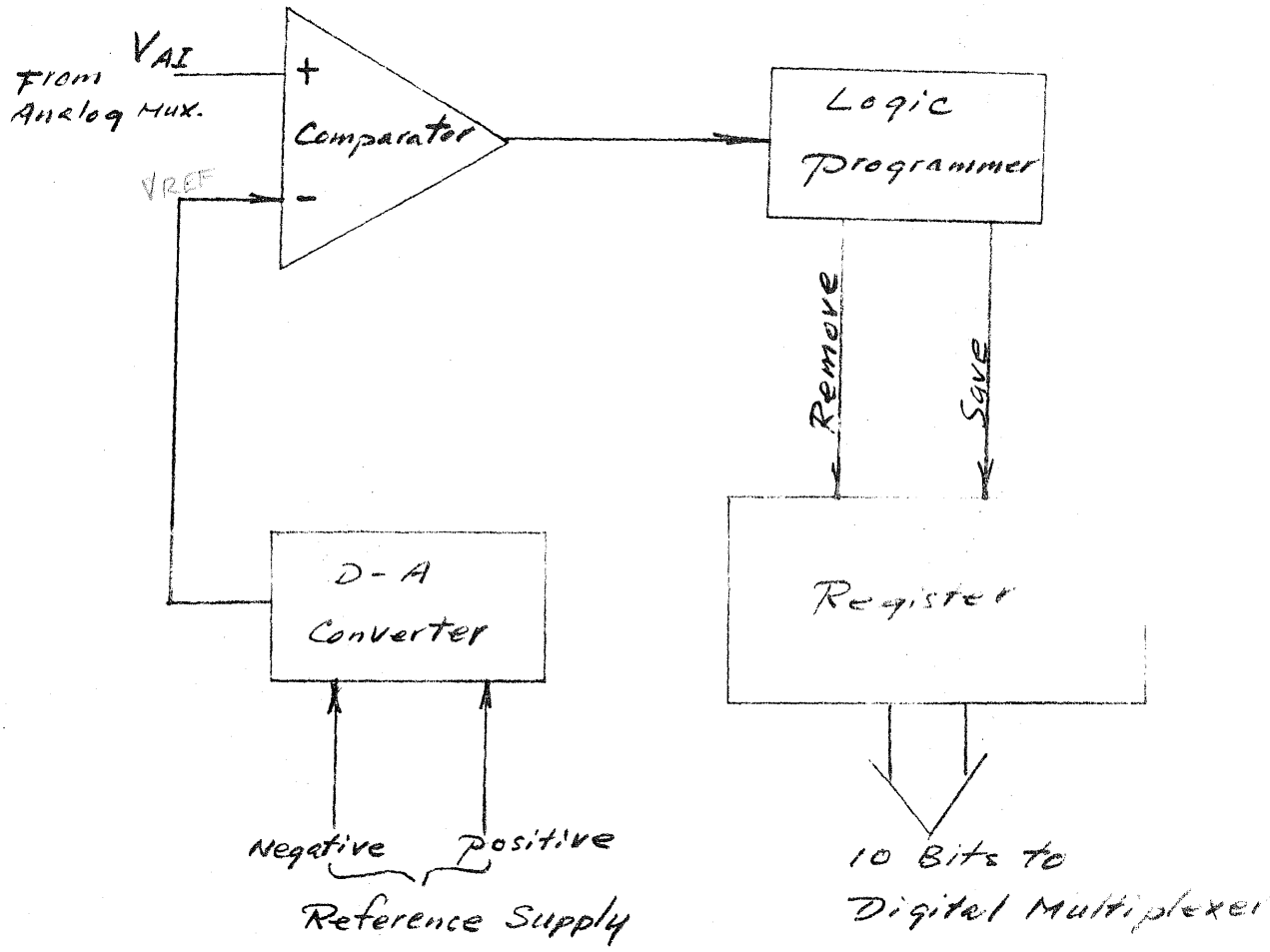


Figure 9-1 Functional Block Diagram - A-D Converter

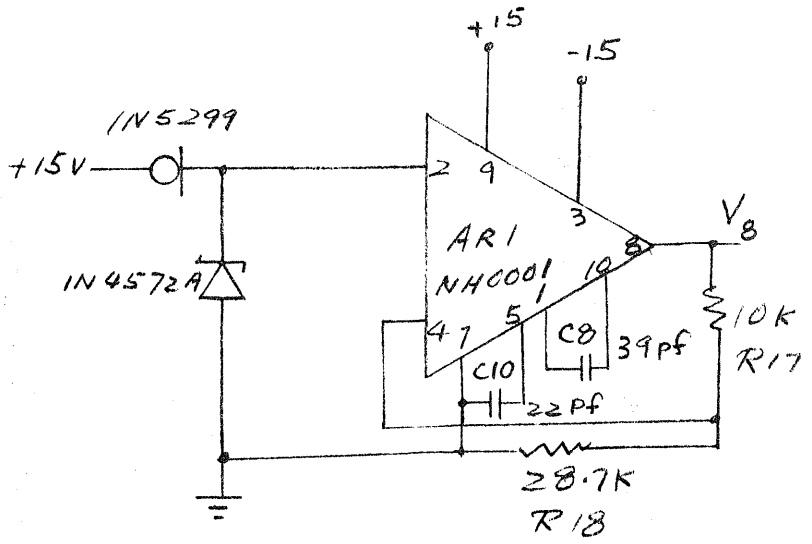


Figure 9-2 Positive Reference Supply

9.1.2.1 Reference Voltage Supplies

A positive reference voltage and a negative reference voltage with good regulation and low drift are needed for D-A converter to generate a variable reference voltage between -10v and +10v, depends upon the input analog signal.

In Figure 9-2, the current regulator IN5299 provides a regulated current 1 2 ma from the +15v supply to the voltage reference diode IN4572A, the voltage at pin 2 (V_2) is well regulated nominally at 6.4 v.

The feedback factor for the NH 0001 is $\frac{R18}{R18 + R17}$

$$V_8 = V_2 \times \frac{R18 + R17}{R18} = 6.4 \times \frac{28.7K + 10K}{28.7K} = 8.64V$$

C_8 and C_{10} are used to prevent potential oscillation in the range of 100KC to 10 MC due to noise.

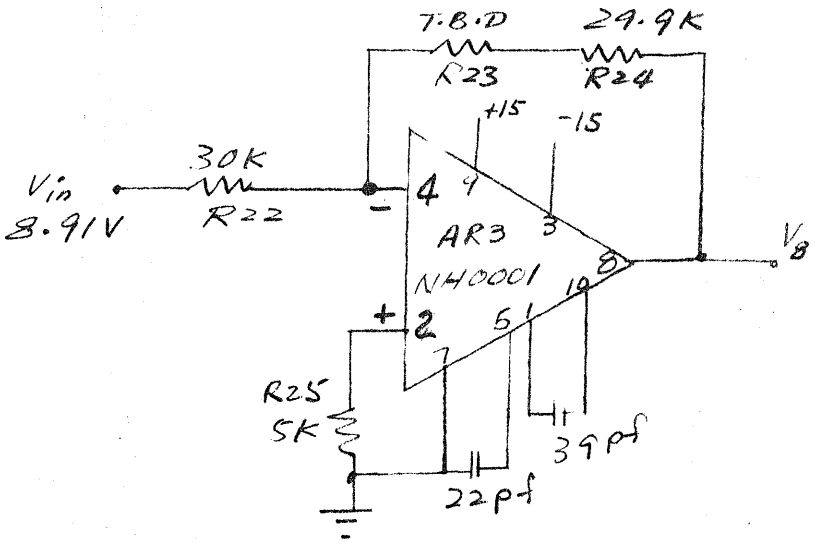


Figure 9-3 Negative Reference Supply

Figure 9-3 shows the negative reference supply, its voltage should track that of the positive reference supply very closely.

The feedback factor for the NH 0001 is $\frac{R22}{R23 + R24}$

$$V_8 = -V_{in} \times \frac{R23 + R24}{R22} = -8.64 \times \frac{R23 + 29.9K}{30K}$$

The value of R23 is to be determined at the test so that V_8 will be made exactly -8.64V.

With R25 = 5K connected to pin 2, the input offset voltage will be limited to less than 1.0 mv.

9.1.2.2 Voltage Comparator

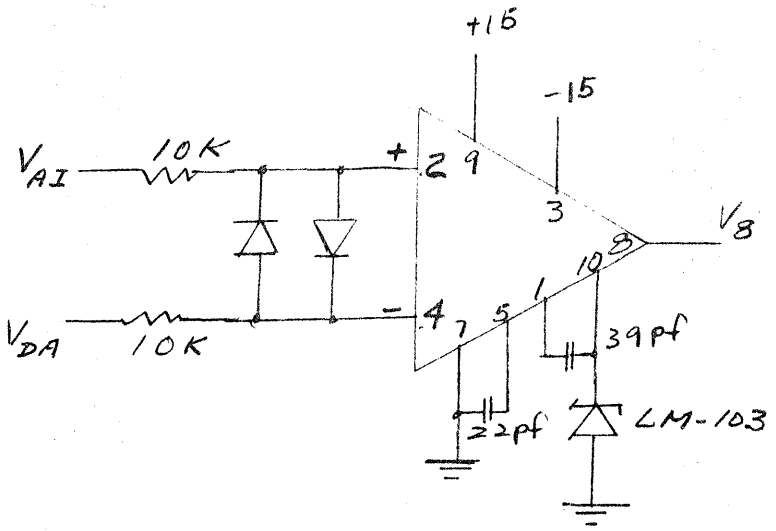


Figure 9-4 Voltage Comparator

Let V_{AI} = Analog input voltage

V_{DA} = Digital to Analog converter voltage or variable reference voltage.

The absolute maximum differential input voltage for NH 0001 is ±7v. Since V2 is 0 volt before it follows V_{AI} to vary, and V_{AI} may range from +10v to -10v, CR1 and CR2 are used to clamp the maximum input differential voltage to 0.7v.

To prevent the output voltage V_8 from exceeding the maximum voltage allowed at 'J' and 'K' input of SN 54L73, VRI (LM 103) is used to clamp V_8 at 5.5 V. This zener diode also clamp V_8 at -0.7v when it tends to swing more negative.

9.1.2.3 Resolution of A-D Converter

The analog input signal ranges from +10v to -10v. Since the entire voltage range is to be converted to a 10-bit digital data, the resolution of the A-D converter is:

$$\frac{20\ V}{(2^{10} - 1)\ \text{states}} = 19.5\ \text{mv per state}$$

Operation of analog gate CDA 2-1

The circuit diagram of 1/2 CDA2-1 is shown in Figure 9-6.

A negative bias voltage is required to keep the analog gate CDA2-1 normally in a depletion mode, so it is cut off. This bias voltage is generated by using the positive reference voltage and Op-amp AR2. Refer to Figure 9-5.

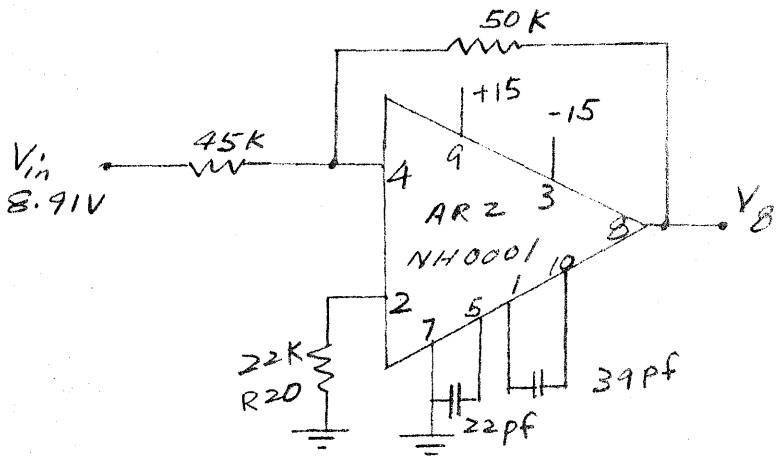


Figure 9-5 Negative Bias Generator

R20 is used to equalize the source impedance looking at pin 4, so that the input offset voltage will be less than 1.0 mv.

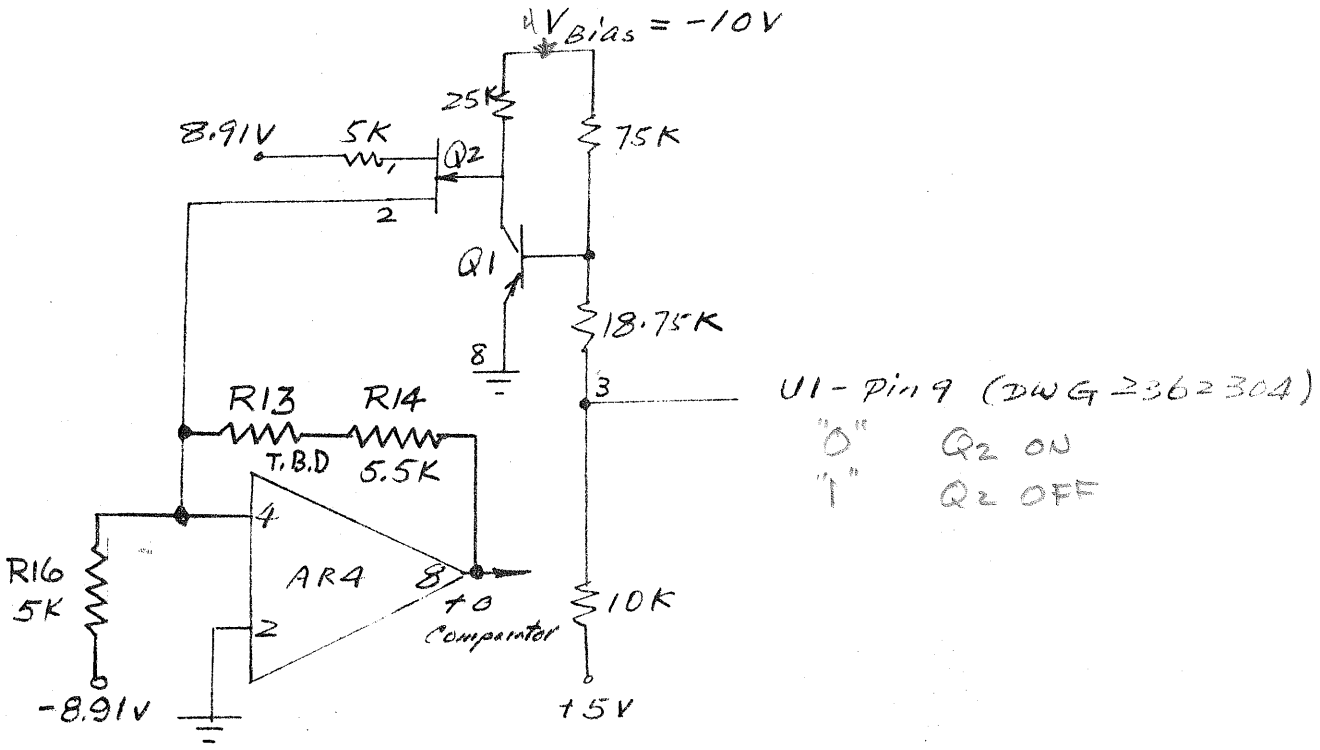


Figure 9-6 Analog Gate

2-5 Operation of Analog Gate CDA 2-1

The circuit diagram of 1/2 CDA 2-1 is shown in Figure 9-6. This is an N-channel FET Switch with its transistor driver. When V_{U1-9} is in '1' state, Q1 is reverse biased to complete cut-off, the negative bias voltage provide V_{GS} = -10V, which keeps FET Q2 cut off. When V_{U1-9} is in '0' state, Q1 is turned on to saturation, thus permitting V_{GS} = 0V, so that Q2 is fully turned on.

3 Operation of the Analog to Digital Converter

State '0' at pin 3 or pin 5 (CDA2-1) is to turn the analog switch on, and state '1' is to turn the analog switch off.

When $V_{AI} > V_{D-A}$ V_8 (AR5) is at state '1'
$V_{AI} < V_{D-A}$ V_8 is at state '0'

Referring to Figure 9-7, as soon as the arriving of the clear/clock pulse (immediately follow the leading edge of data demand) flip flops U1, U2, U3, U7 and U9 are all cleared. The states that drive the analog switches and that present at the output of the A-D converter are:

	(MSB)									(LSB)
Bit	10	9	8	7	6	5	4	3	2	1
	Q	$\overline{Q}$	$\overline{Q}$	$\overline{Q}$	$\overline{Q}$	$\overline{Q}$	$\overline{Q}$	$\overline{Q}$	$\overline{Q}$	$\overline{Q}$
State drive analog switches	0	1	1	1	1	1	1	1	1	1
	$\overline{Q}$	Q	Q	Q	Q	Q	Q	Q	Q	Q
State present at the output	1	0	0	0	0	0	0	0	0	0

This driving state implies $V_{D-A} = 0$

Under this condition, the comparator output $V_0 = 0$.

Assume following the clear of all flip-flops, $V_{AI} = -22$ mv

Since $V_{AI} < V_{D-A}$ therefore V_0 = '0'

$J_{10} = K_{10}$ = '0'

$J_9 = 1$ K9 = K8 = - - - - - K1 = 0

As soon as the clock arrives, Q10 stay unchanged, Q9 toggles to 1, $\overline{Q}$9 disables the next clock pulse to bit-10.

$\overline{Q}$9 = 0 throws the 10k Ω resistors into the summing network.

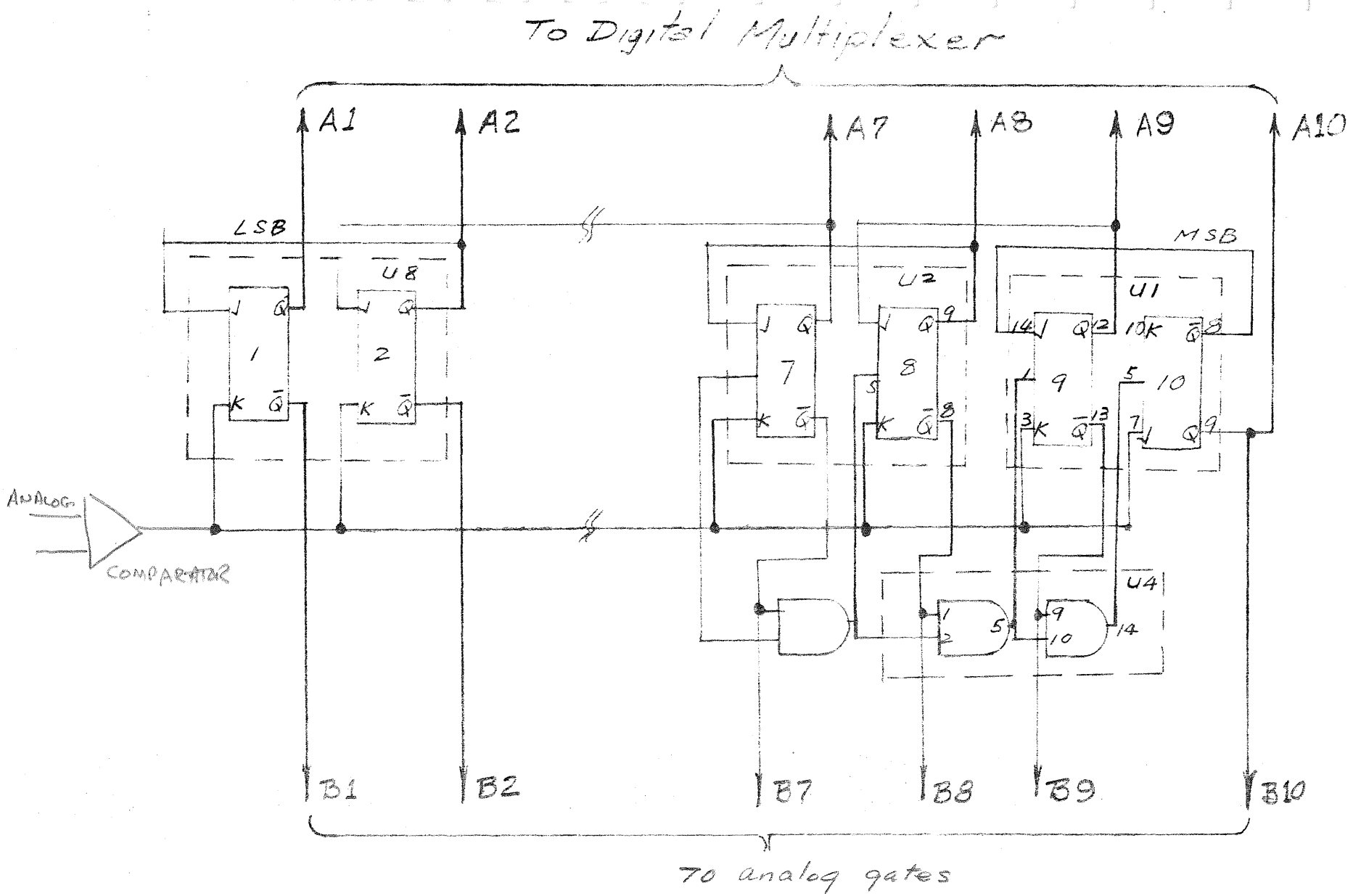
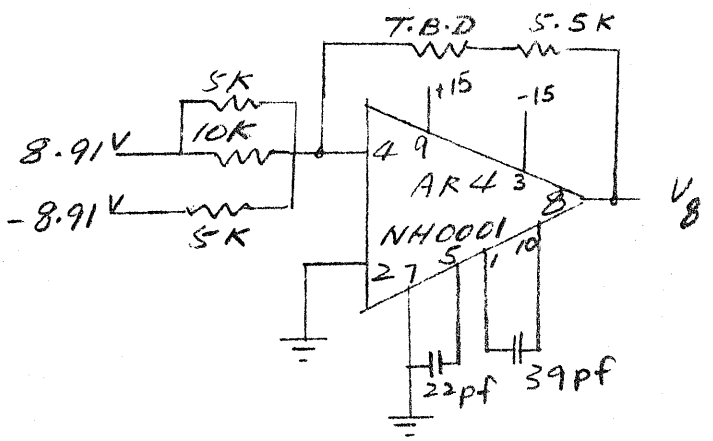


Figure 9-7 Sequence of Operation, A-D Converter



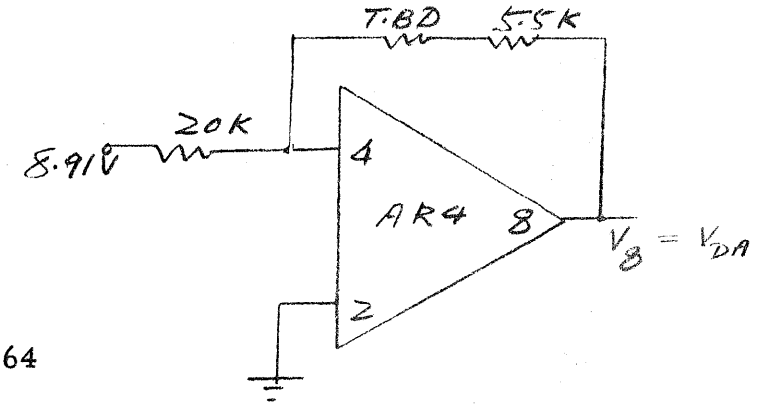
Now $V_{DA} = V_8 = \frac{-5.5K}{10\ K} \times 8.64V = -4.75$

Therefore $V_{AI} > V_{DA}$, V_0 = '1'

J10 = J9 = J9 = J8 = 1 J7 = J7 = J6 = ---- J1 = 0

K10 = K9 = --- K1 = 1

When the clock pulse arrives at bit 8 and bit 9, $\overline{Q}_9$ toggles to 1 to turn off the analog sw for bit 9, Q_8 toggles to 0 to turn on the analog sw for bit 8. As a result of the above switching, the 10kΩ resistor is taken out and the 20k resistor is thrown into the summing network.



$V_{DA} = \frac{-5.5K}{20K} \times 8.64$

= -2.45V

= -2.37V

again $V_{AI} > V_{DA}$, V_o = '1'

$\overline{Q}_8$ = 0 disables the next clock to bit 9 and bit 10

J10 = J9 = J8 = J7 = 1 J6 = J5 = - - - - - J1 = 0

K10 = K9 = ---- K1 = 1

When the clock pulse arrives at bit 7 and bit 8, $\overline{Q}_8$ toggles to '1' to turn off analog sw for bit 8.

$\overline{Q}_7$ toggles to '0' to turn on the analog sw for bit 7. As a result of the above switching, the 20kΩ resistor is switched out and the 40k Ω resistor is switched into the summing network.

$$V_{DA} = \frac{-5.5K}{40K} \times 8.64 = -1.186V$$

Again $V_{AI} > V_{DA}$, V_o = '1'

The process is successively tried until $\overline{Q}_2$ toggles to '1' and $\overline{Q}_1$ toggles to '0' which takes the 1.28 MΩ resistor out of and the 2.56 M Ω resistor into the summing network.

$$\text{Then } V_{DA} = -\frac{5.5K\,\Omega}{2.56M\,\Omega} \times 8.64$$

$$= -21.5 \text{ mv}$$

Now $V_{AI} < V_{DA}$ V_0 = '0'

J9 = ---- J2 = 1 J10 = J1 = 0

K9 = K8 = ---- = K1 = 0

Q1 = 0 disables nextclock to all more significant bits (as long as one sampling word is concerned, 10 shift pulses have been over, without the gating of data demand there will be no more clock pulse to come).

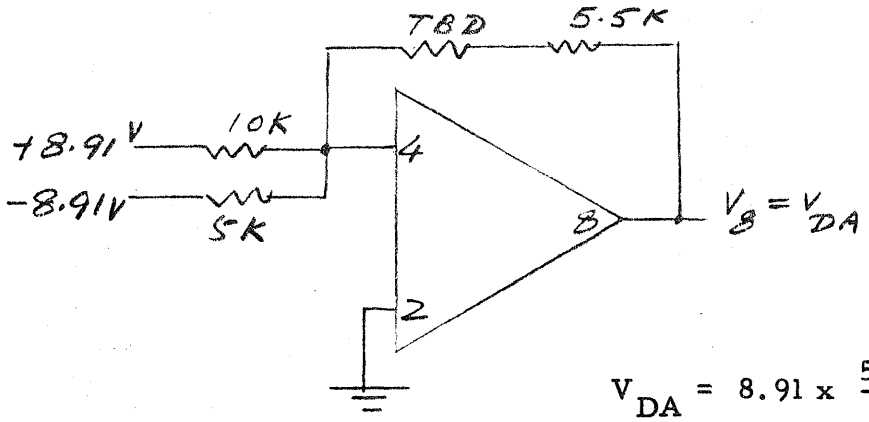
The output of the A-D converter settles at 1 0 0 0 0 0 0 0 0 1 which is a conversion of -22mv analog input signal.

For another illustration, assume $V_{AI} = +10v$

Since $V_{DA} = 0$, then $V_{AI} > V_{DA}$ hence $V_0 = '1'$

J10 = 1 J9 = 1 K9 = K8 = ----- K1 = 1

When the clock pulse arrives at bit 10, Q_{10} toggles to '1', which throws the 5kΩ resistor out, $\overline{Q}_9$ toggles to '0' which throws the 10kΩ resistor in and disables next clock pulse to bit 10. As a result of these,



$$V_{DA} = 8.91 \times \frac{5.5K}{5K} - 8.91 \times \frac{5.5K}{10K}$$

$$= 8.91 \times \frac{5.5K}{10K} = 4.9V$$

Again $V_{AI} > V_{DA}$, $V_0 = '1'$

J10 = 1 J9 = 0 J8 = 1

K9 = K8 = K7 = --- K1 = 1

When the clock pulse arrives, bit 9 toggles with $\overline{Q}_9 = 1$, $\overline{Q}_8$ toggles to 0 which throws the 20kΩ resistor into the summing network, and disables the next clock pulse to bit 9 and bit 10, as a result of these,

$$V_{DA} = 8.91 \times \frac{5.5k}{10k \;//\; 20k} = 8.91 \times \frac{5.5k}{6.68k} = 7.12v$$

again $V_{AI} > V_{DA}$ $\quad V_0 = '1'$

J10 = 1 J9 = J8 = 0 J7 = 1

K9 = K8 = K7 = ------ K1 = 1

The process repeats successively until the last clock pulse arrives, $\overline{Q}_1$ toggles to 0 which throws 2.56 MΩ resistor into the summing network

now $V_{DA} = 8.91 \times \frac{5.5k}{5k} \simeq 10v$

since $V_{AI} = V_{DA}$ therefore $V_0 = '0'$

The conversion process finally settles at the A-D output state 0 0 0 0 0 0 0 0 0 0 which indicates an analog input voltage +10v.

SECTION 10

LSG ASSEMBLY 236 2127

10.1 POWER CONVERTER

10.1.1 General Description

The Power Converter of the LSG, performs the following functions:

1. Regulates the input power.
2. Isolates LGE signal return from the ALSEP CPU Power Return.
3. Converts the ALSEP voltage to the voltages required by the LSG.
4. Isolates high frequency LSG transients from the ALSEP Power lines.
5. Provides signal drive for the Instrument Heater regulator.

To accomplish these functions the Power Converter utilizes a Regulator which feed a DC/DC Converter as shown in Figure 10-1. The Converter outputs are rectified and filtered. Included with the power outputs is a filtered square wave signal which is utilized by the Instrument Heater regulator as the synchronizing input drive.

10.1.2 Circuit Description

10.1.2.1 Regulator

The Regulator conditions the input power voltage, ALSEP 29VDC, and provides to the DC/DC Converter a regulated voltage, 26.6 VDC nominal. The configuration shown in figure 10-2 includes a class-A regulator pass element within a DC amplifier feedback loop which maintains the output at the reference voltage V_R times the feedback ratio.

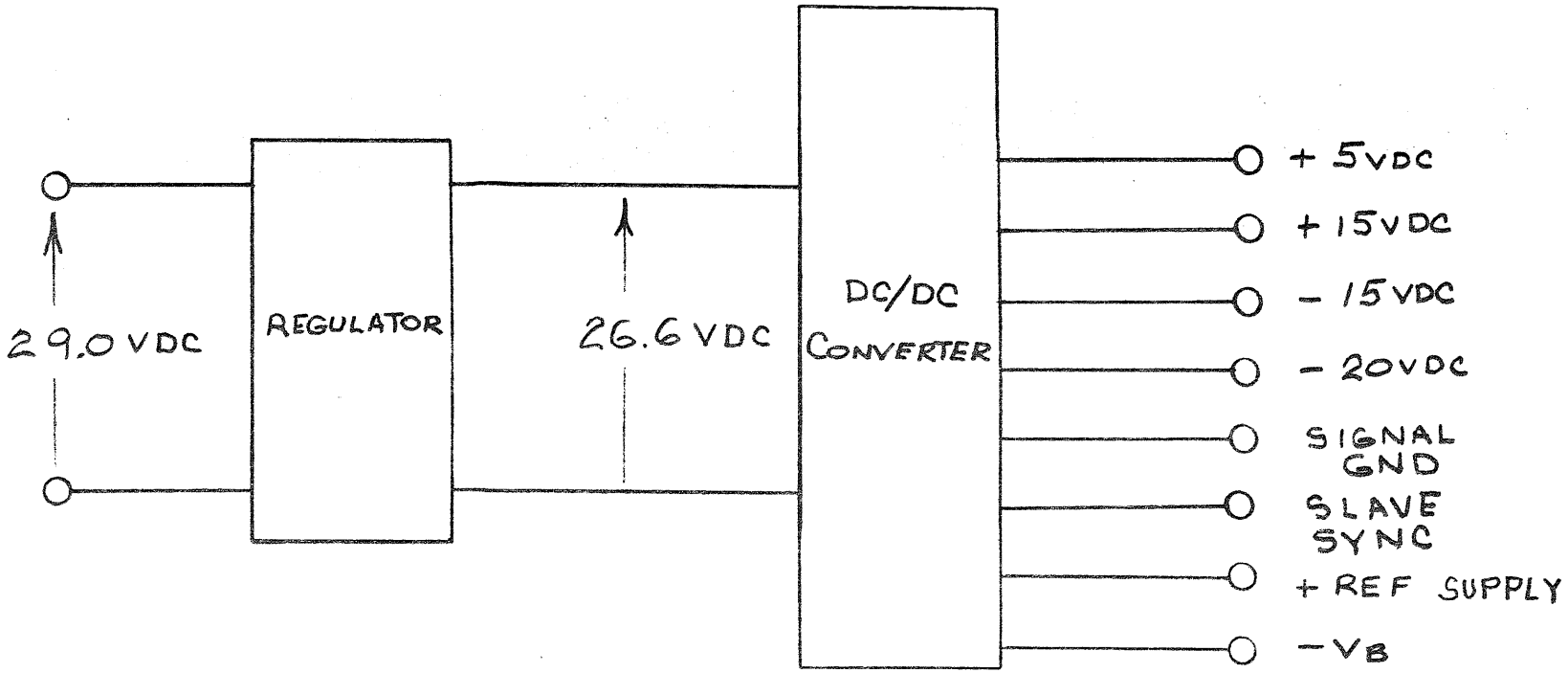


Figure 10-1. Power Converter

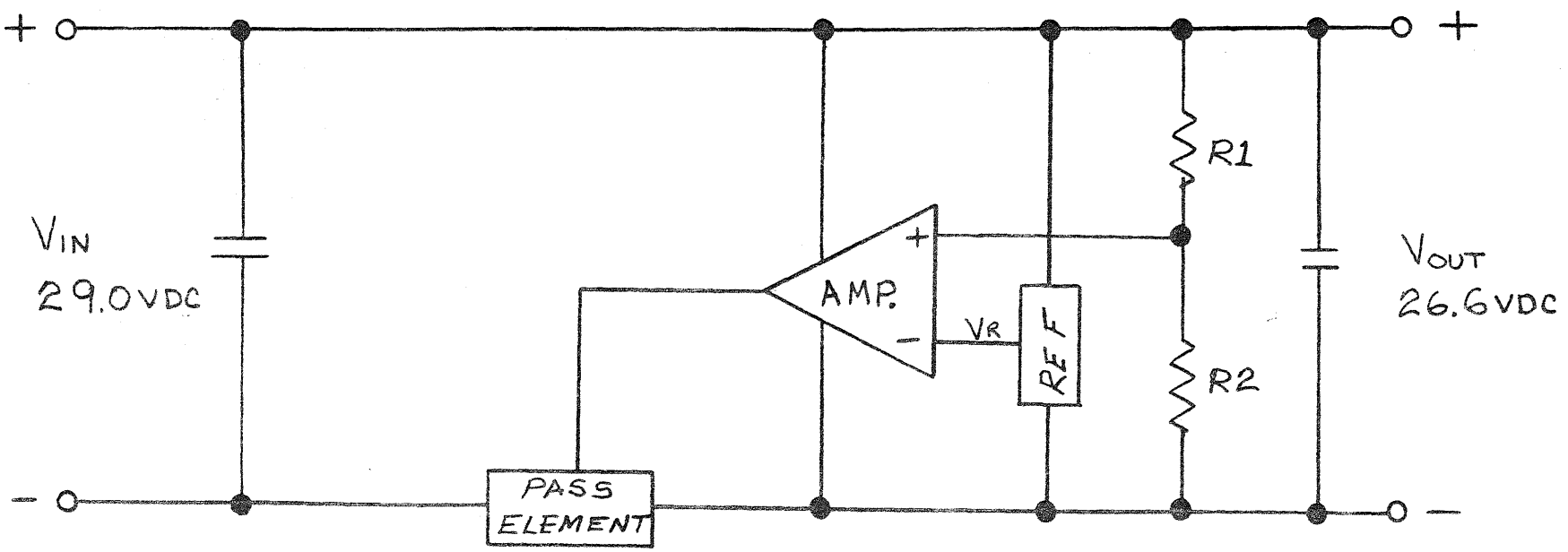


Figure 10-2. Regulator - Class-A

$$V_{OUT} = V_R \frac{R_2 + R_1}{R_1}$$

The open loop voltage gain, A_{OL}, is approximately

$$A_{OL} = 70 \text{ db}$$

and the feedback ratio β is nominally

$$\beta = .24$$

for a $V_R = 6.4$ volts.

The pass-element, Q_4, is a NPN high gain transistor operating in the high efficiency grounded emitter configuration. The amplifier is a three stage discrete component configuration and is utilized in lieu of an integrated circuit for the reason of the increased power efficiency that can be achieved in this approach. The reference zener is a 1N4568A low current diode biased at approximately 100μa and hence comprises a large portion of the Regulator NO LOAD Power. This NO load bias current is approximately 330 μ a, yielding a total of 9.5 MW of power, or approximately .4% of the nominal LSG command mode input operate power, which is approximately 2500 MW.

The efficiency of the Regulator is constant to ± 2% for input power levels in excess of 500 MW and is given approximately by the following expression where Pwr In is input power:

$$\text{Eff} = \frac{V_{OUT}}{V_{IN}} \left[1 - \frac{9.5 + .01 P_{WR\ IN}}{\text{PWR IN}} \right] \times 100\%$$

For a power in level of 2500 mw the Regulator Efficiency is

$$\text{REG. EFF.} = 90.5\%$$

The regulator output variation is approximately +. 3% for a load variation from 15% to 150% of the command mode load. The line regulation is approximately . 15% for a 10% input voltage variation.

The turn-on/off time of the regulator is approximately 1. 5 MS as measured from 10% to 90% of the output voltage for a step input of the ALSEP 29 volts.

The setting of the output voltage to compensate for component variations, particularily zener variations, is accomplished by the selection on resistors R3 (1%) and R7 (. 5%) which include a selectability range of 5% and 3% respectively to allow for the nominal setting of the 15V converter output to within 1% under nominal command mode load. This technique of voltage adjustment was selected over a potentiometer for the reason of greater reliability of the resistor over the potentiometer. There will be no need for further adjustment after the initial setting.

10. 1. 2. 2 Converter

The DC/DC converter is a Jensen configuration (two transformer circuit) and is shown in figure 10-3. This configuration is utilized in lieu of the Royer circuit (single transformer circuit) for the following reasons:

1. Increased power efficiency and greater reliability -lower transistor dissipation during the switching times and less second breakdown stress on these devices.

2. Decreased EMI generation-absence of low saturation impendences in the output transformer results in lower conducted EMI to the extent of approximately 100 times.

The feedback transformer T1 and the output transformer T2 both utilize Magnetics Inc supermalloy type miniature cores which exhibit extremely low excitation power characteristics. The feedback transformer is designed to saturate at 36 μ s yielding a maximum flux density in the output transformer of 65% capacity. Circuit oscillation frequency is 14 KC nominal and will remain stable to within 3% of its initial frequency following regulator voltage setting.

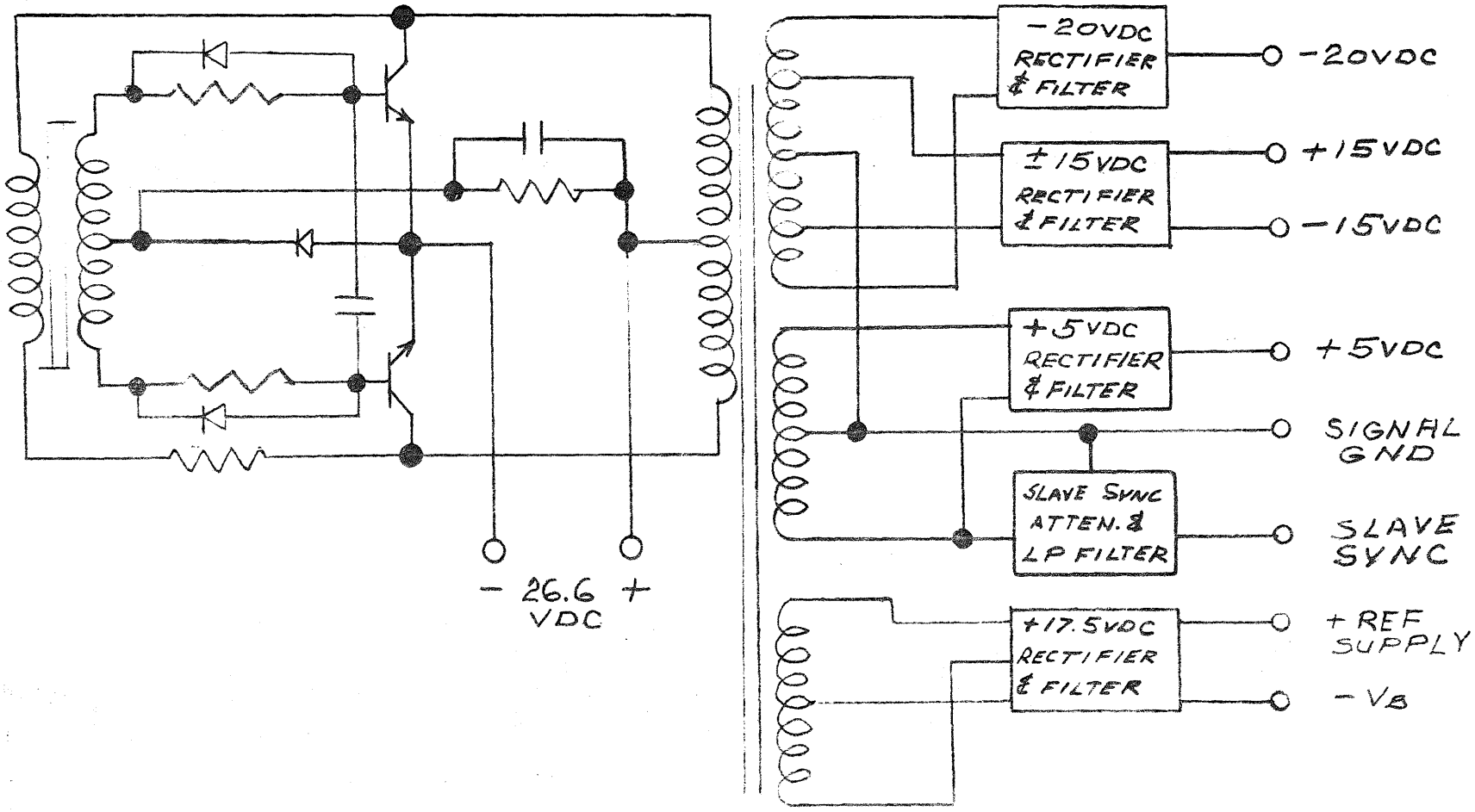


Figure 10-3. Converter/Rectifier

The converter power outputs with respect to signal ground are:

1. +5 VDC
2. +15 VDC
3. -15 VDC
4. -20 VDC
5. 17.5 VDC Floating (+ Ref Supply $-V_B$)

Each of these outputs are generated by a full-wave rectifier and capacitive filter from the output transformer centertap grounded secondary. Output voltage variation as a function of the input ALSEP 29 volts is approximately the same as the regulator variation which is:

LINE REG. = .15%

for a 10% change in the input voltage.

10.1.2.3 Load Regulation

Output voltage variation for a 10% load change and the output ripple at nominal load are given below.

	Converter Variations/ Δ load	Ripple
+5VDC	.4%	.1VP-P
+15VDC	.25%	.07VP-P
-15VDC	.15%	.08VP-P
-20VDC	.2%	.05VP-P
E_o REG.	< .1%	.12VP-P
E_{in} REG (ALSEP 29V)	N/A	.04VP-P

10.1.2.4 Slave Sync

The Slave Sync Signal is generated from the 5 volt power winding and imparts a balanced load to this winding. This 11.8 VP-P squarewave signal is attenuated to 7 VP-P to a 3db break frequency of 45 KC where it is further attenuated at a rate of 20 db/decade to reduce high frequency coupling in the cabling to the slave heater circuit. The rise and fall times are identical and approximately 7.5 μ. s.

10.1.2.5 Ground Decoupling

The Power Converter performs AC decoupling of the 29V input return and chassis ground to the Signal Ground at the PC board by means of 1 μ. f. CKR06 capacitors. This decoupling includes the EMI cover which encloses the Power Converter components since the cover is electrically connected to the 29V input return.

SECTION 11

LSG ASSEMBLY 2362182

11.1 FIXED GAIN PRE-AMPLIFIER

11.1.1 General Description

The Fixed Gain Pre-amplifier serves to couple the sensor center plate to the electrostatic loop electronics with minimum electrostatic loading of the sensor. It also provides a sufficient amount of gain with low noise to make the noise contribution of the post amplifier negligible.

11.1.2 Circuit Description

The carrier frequency unbalance voltage, developed at the sensor center plate when the sensor center plate is displaced from electrical null, is capacity coupled to R2 at the amplifier input by C5 (refer to figure 11-1). C5 also blocks the d-c voltage developed by the bias current across R2 from the sensor. R1 provides a d-c return for the sensor center plate.

The amplifier is a non-inverting circuit with a closed loop gain of 40. The resulting input impedance of the amplifier is sufficiently high so the loading of the sensor at carrier frequency is determined entirely by R1 and R2 shunted by the capacitance of the line length which couples the sensor to the amplifier input. The pre-amplifier is located inside the sensor heater box to minimize this line length. C6 is provided if necessary to equalize the voltage transfer from sensor output to amplifier input if this line capacitance should vary from sensor to sensor.

Frequency compensation capacitor C7 provides power supply noise rejection and minimizes phase shift in the pre-amplifier at carrier frequency.

R3, R4, C8 and C9 provides a low Qband-pass filter around the carrier frequency. The gain at the low end of the carrier frequency is reduced to near unity by C9 and at the high frequency by C8.

Additional noise rejection of approximately 50 db from the power supply noise is obtained by R5, R6, C1, C2, C3 and C4. This is necessary to overcome the power supply noise that may be impressed on the low level seismic signal.

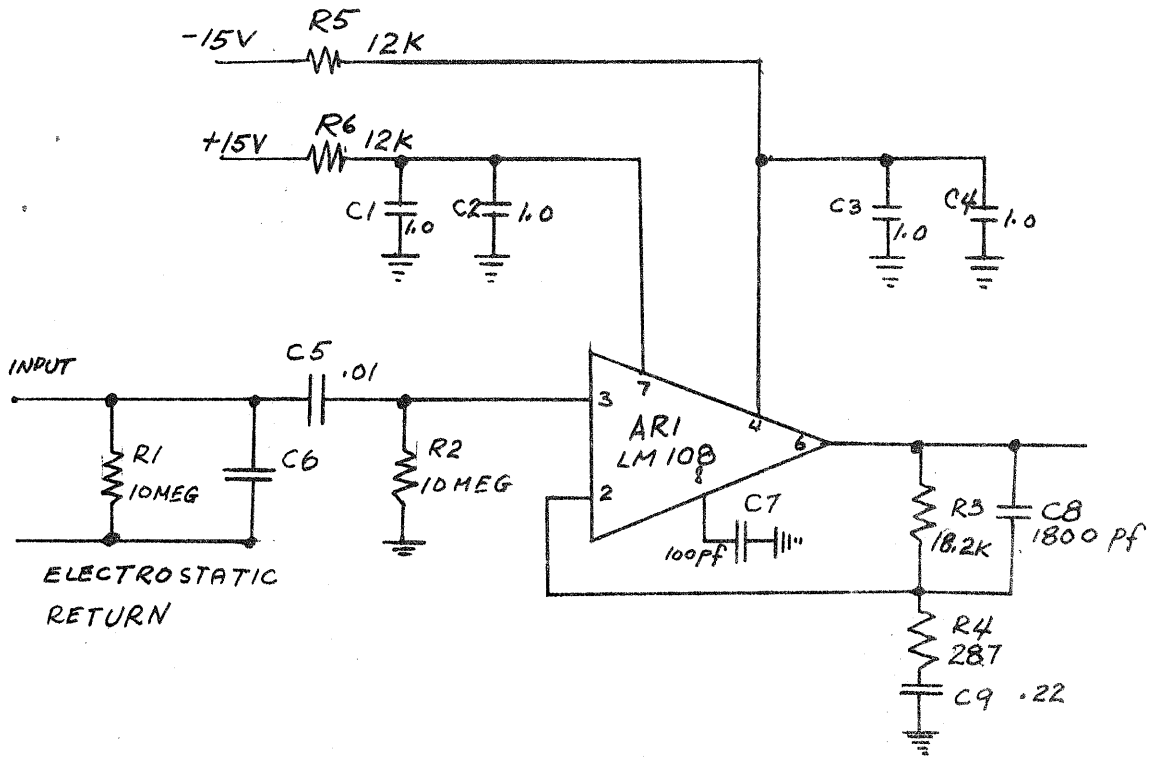


Figure 13-1 Fixed Gain Pre-Amplifier

SECTION 12

LSG ASSEMBLY 2362370 & 2362076

12.1 THE SHAFT ENCODER ELECTRONICS

12.1.1 General Description

12.1.1.1 The Encoders

The system is equipped with Librascope, Model 719-11-5, 19 bit shaft encoders.

Each shaft encodes is designed with two sets of brushes. One set of 19 advanced brushes and a set of 19 retarded bursches.

The rotating part of the encoder is made up of three disks which have been geared together--reduced 64:1. A printed circuit board is bonded to the disk. The printed circuit board consists of an etched code of conducting and non-conducting surfaces, which is representative of mechanical shaft position in binary form. There are certain areas on the surface of the printed circuit board where it is possible to have simultaneous brush contact between bits at the point of transition. Errors in shaft position will be present at all points of transition to a more significant bit.

In the dual brush system, the advanced and retarded brushes operate from independent tracks on the printed circuit board. These tracks are designed so the points of transition and the brushes are displaced with respect to the position of the printed circuit card. Ambiguity can be avoided by selecting the opposite track before the point of transition. This selection is made in the electronic read out system.

12.1.1.2 Shaft Encoder Logic Circuit

The shaft encoder electronics logic must select the correct track for each bit based on the state of the previous bit. To avoid ambiguity, at the point of transition, alternate tracks are sampled in the following manner: If the output of the previous bit is high, the advanced brush is selected. If the output of the previous bit is low, the retarded brush is selected.

Two shaft encoders are used in the system. One encoder is coupled to the course screw shaft which is designated as encoder "A." The other shaft encoder is coupled to the fine screw servo shaft. This encoder is referred to as encoder "B."

It is necessary for the shaft encoder electronics to multiplex data from shaft encoders, "A" and "B." The output data word is 10 bits. The shaft encoder electronics is designed to separate the 19 bit word; into two 10 bit words for each shaft encoder. Refer to Table 12-1.

A two bit binary counter in the shaft encoder electronics is preset on the frame mark and clocked on each data demand pulse. Refer to Figure 12-2. During the first two data demand pulses, the course encoder is addressed by the shaft encoder electronics. The next two data demand pulses will address the fine encoder. This is implemented with two power gates, which are driven from the two bit counter. Each power gate is used to drive the common input to the shaft encoder.

The binary counter and the power gates are wired for the following output sequence: Refer to Table 12-1.

TABLE 12-1 Shaft Encoder Electronics Output Sequence

Sequence	U2-12(14A2) U2-9 (14A2)	Word	Encoder	Function
1	0 0 (reset)	1st Word	Coarse Encoder	9 most significant bits
2	0 1	2nd Word	Coarse Encoder	10 least significant bits
3	1 0	3rd Word	Fine Encoder	9 most significant bits
4	1 1	4th Word	Fine Encoder	10 least significant bits
5	0 0	5th Word	Coarse Encoder	9 most significant bits
6	etc.			

Each 10 bit word is loaded into the multiplexer at the leading edge of the clear/clock.

12.1.2 Circuit Description

Drawings 2362370, and 2362076 will be used as a reference in the following circuit description. Component designations below refer to items of board 14A2, assembly 2362076, unless otherwise noted.

Refer to Figure 12-1.

Flip flops UIA & B, and Q1 & Q2, make up an electronic switch which will respond to the proper commands and signal conditions to switch the shaft encoder power. Table 12-2 will list the commands and signals to the shaft encoder electronics with the response to these signals in their correct order.

TABLE 12-2 Plus 5 Volt Power Sequence

Read Shaft Encoder Card	Flip flop UIA is preset. J-K inputs of UIB are enabled.
First 90th Frame Pulse Following Read Command	UIB is toggled. Pin 8 will go high. Q1 and Q2 will switch on. +5 volt power is now supplied to all logic on board 14 A1 & A2. J-K inputs of UIA are enabled.
2nd 90th Frame Pulse	UIA & B are toggled. Q1 and Q2 will switch off, removing +5 volts from the remainder of the logic. UIA & B are reset pending the arrival of a read command pulse.

Upon arrival of a frame mark at the input of U7-A, counter U2A & B is reset. Refer to Table 12-1. In the reset state pin 8 will go high to enable gates which switch bits A10-A18 for loading into the multiplexer.

At this time U2-13 will go high which will provide a low output at power gate U3-10. Power gate U3-10 will ground the common to encoder "A." This will enable encoder "A," 19 advanced, and 19 retarded outputs to the encoder electronics.

On the schematic drawings (2362373, and 2362079) - "Aa4 38" is referring to the input (on the encoder electronics board) which is wired to "A" encoder, the Advanced brush, bit number 4, pin 38 on the printed circuit board. Similarly, Br 5 44, is referring to the input connected to "B" encoder, the retarded brush, bit number 5, pin 44 on the printed circuit board.

If A0 is low, U13-8 (14A1) will be high which will enable the retarded brush of A encoder, bit 1. If Ar 1 is low, U14-8 (14A1) will be high which will enable the retarded brush of A encoder, bit 2. If Ar2 is high, U10-8 will be high which will enable the advanced brush of A encoder, bit 3. This system is propagated down thru A_{18}.

Upon arrival of the trailing edge of the first clear/clock pulse U2A & B will switch to state 01. Refer to the 2nd sequence of Table 12-1. At this time U2-9 will go high. This will enable gates which control bits A0-A9 for loading into the multiplexer.

On the trailing edge of the 2nd clear/clock pulse, counter U2A & B will switch to the 10 state. Power gate U3A will pull the common on shaft encoder B to ground. This will enable the 38 output lines, or 19 retarded plus 19 advanced input lines to the encoder electronics board. At this time U2-8 will go high. The input to gates which control bits B10-B18 will be enabled.

On the trailing edge of the 3rd clear/clock pulse counter U2A & B will switch to the 11 state. The output of U2-9 will go high. This will enable gates which control bits B0-B9. Bits 1-10 are the last 10 bits of the fine encoder--line 4 in Table 1. The words are repeated until the 90th frame pulse--when the encoder power is switched off by U1.

1. Command read pulse in presets U1-2 (pin 1 on board) enables J-K 7, 10 inputs

2. J-K 7, 10 inputs

3. J-K 3, 14 inputs +5 volts switched, Q_2 collector

4. 90th Frame Pulse Pin 9 on board 14A2

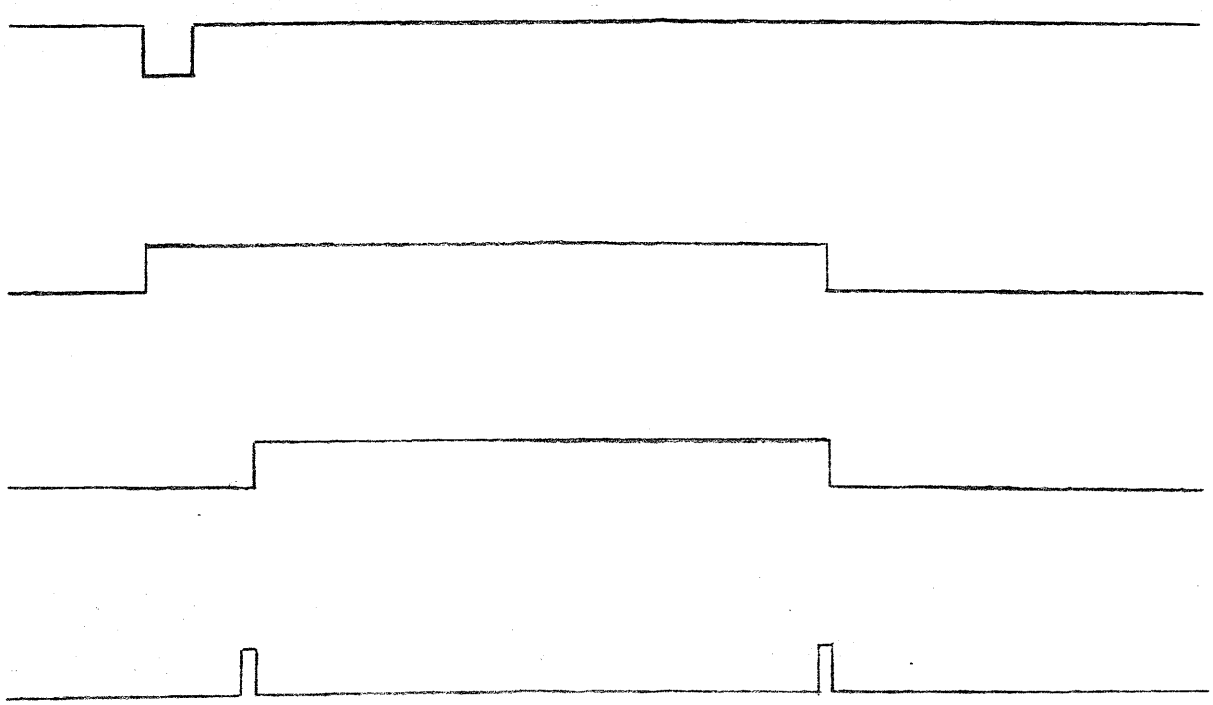


Figure 12-1 +5 Volt Switched Timing Diagram

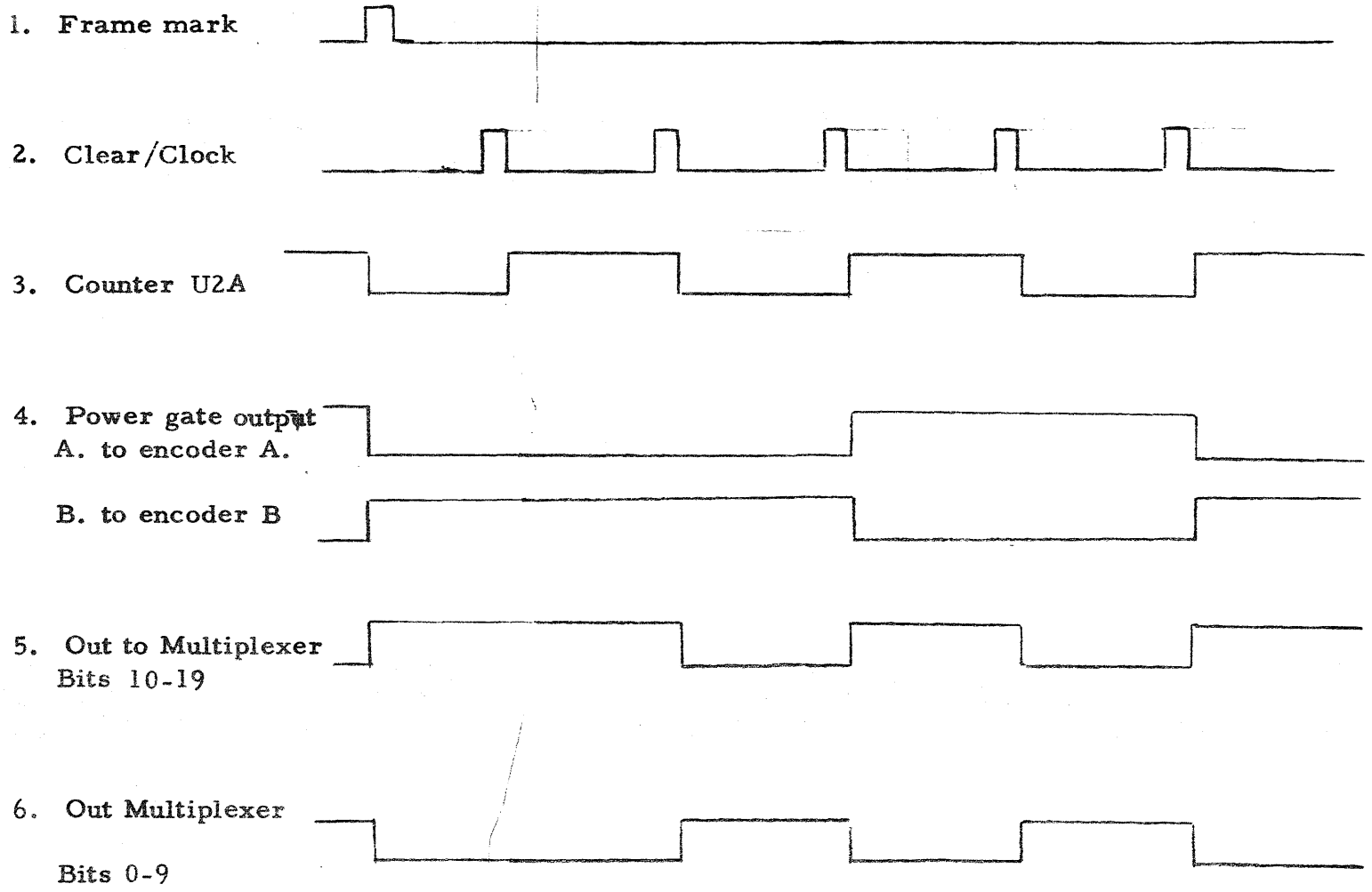


Figure 12-2 Shaft Encoder Timing Diagram

SECTION 13

LSG ASSEMBLIES 2362378 & 2362382

13.1 SENSOR TEMPERATURE MONITOR CIRCUIT

13.1.1 General Description

The purpose of the temperature monitor is to give an analog indication of the temperature of the sensor spring. This indication is required because the heater box heater must be adjusted to maintain the spring at its inversion temperature and the monitor output is a verification that this control is being held.

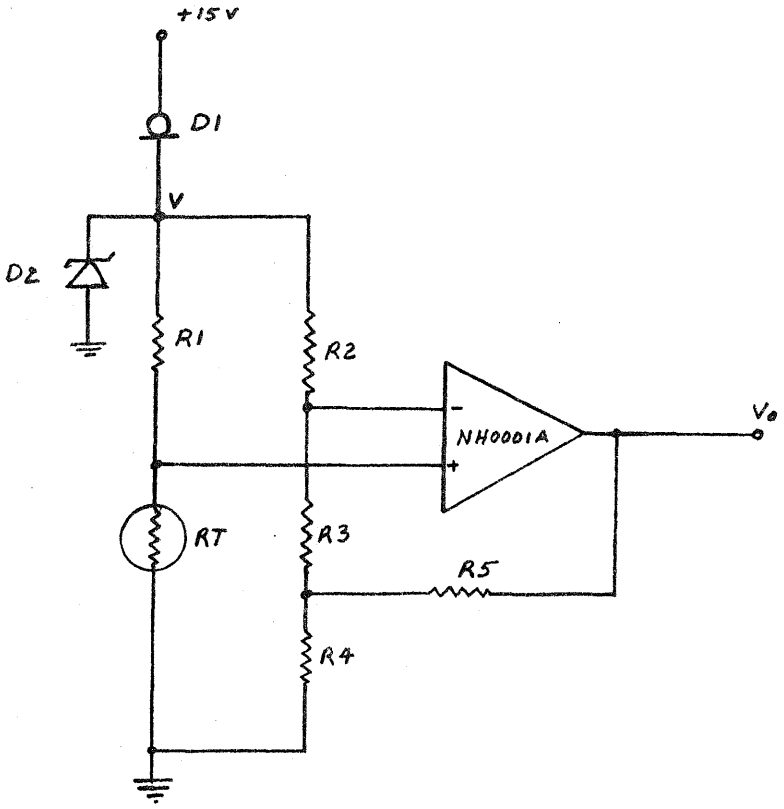
13.1.2 Circuit Description

A simplified schematic with its transfer function is shown in figure 13-1. The monitor circuit consists of a thermistor bridge circuit with an operational amplifier on the output, resulting in an approximately linear output voltage proportional to thermistor resistance. The thermistor resistance varies inversely with temperature. R3, shown in figure 13-1, will be selected to match the circuit to the inversion temperature of each individual sensor spring, so the full useful range of the circuit can be utilized. The output of a temperature monitor circuit using a YSI 44032 thermistor and circuit values selected to center the monitor range at approximately 50 ^{o}C is shown in figure 13-2.

The bridge circuit consists of a pair of current source resistors, one supplying a YSI Thermistor of approximately 10K Ω and the other supplying a fixed resistance with a feedback tap. A National Semiconductor Type NH0001A operational amplifier is connected differentially to the bridge circuit and the feedback is calculated to cover approximately a $\pm$ 2 ^{o}C range for a +10 volt output. The NH0001A has been selected for this application because of its extremely low power drain in addition to its good performance. To set up a stable bridge supply voltage, a 6.4 volt temperature compensated zener diode is driven by a 1/2 milliampere, field effect current regulator diode. One percent metal film resistors are used throughout the circuit for stability and reliability. The board that the circuit is mounted on is attached to the heater box so that the stable temperature environment will improve the accuracy of the circuit.

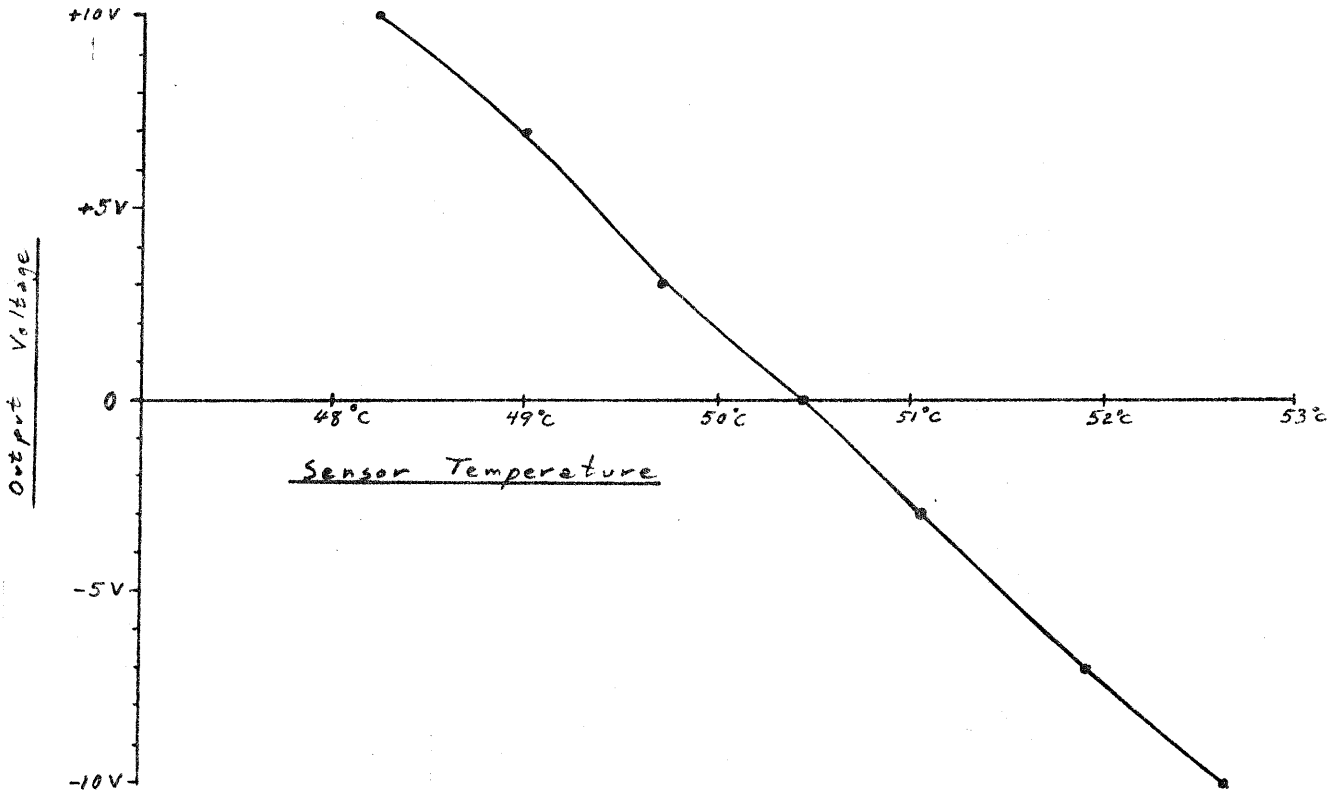
In the range of V_o between -10 and +10 volts the following equation is a good approximation of the transfer function of this circuit.

$$V_o = \frac{VR_5 (R_T - R_3 - R_4)}{R_4 (R_2 + R_T)}$$



$R_1 = R_2$

Figure 13-1 Sensor Temperature Monitor Circuit



Sensor Thermistor Calibration Curve
Figure 13-2

13.2 HEATER BOX HEATER CONTROLLER

13.2.1 General Description

In order to maintain the sensor spring at its inversion temperature within $\pm$ .001°C, the sensor assembly is mounted within a heater box which has a heater winding uniformly wrapped on it. A linear type control system is utilized to maintain this control. The control system consists of an adjustable thermistor bridge circuit driving a high gain amplifier with a power output stage controlling the heater current. The thermistor bridge circuit is adjustable through sixty four .05°C steps through combinations of six relay commands. This adjustment capability is required so that the sensor spring temperature can be adjusted to its inversion temperature in its remote environment in case it should change slightly with time or handling.

13.2.2 Circuit Description

A simplified schematic of the control system is shown in figure 13-3. The bridge circuit consists of two equal current legs, one with a YSI Thermistor of approximately 10 kΩ and one with a selected resistor (R_3) to center the control range on the sensor spring inversion temperature and a resistor ladder network ($R_4 \rightarrow R_9$) in combination with relays K1 thru K6 which is designed to give sixty four .05°C steps of heater box temperature. A field effect current regulator diode is used as a supply for the bridge circuit. A National Semiconductor NH0001A is used to sense bridge imbalance and it in turn drives a 2N2060 differential amplifier which drives two PNP transistors connected in Darlington configuration.

The circuit and parts used have been selected to obtain high gain, and yet low dissipation to eliminate extraneous heat sources within the instrument housing. The final transistor output stage is mounted remotely on board #6 in the electronics package to eliminate the possibility of creating a hot spot which could disturb the heater box temperature stability. The supply voltages for this circuit are regulated +20 & +10 volts which are supplied by regulator circuits for the Instrument Heater control in the electronic package with a return to the heater voltage return. The circuit is mounted on the heater box assembly to provide a temperature stable environment in order to achieve the accuracy required.

The controller gain will drive the heater from a completely on to completely off condition with approximately a 10 Ω change in thermistor resistance. This corresponds to a .025°C change in temperature with a YSI 44032 thermistor at 50°C.

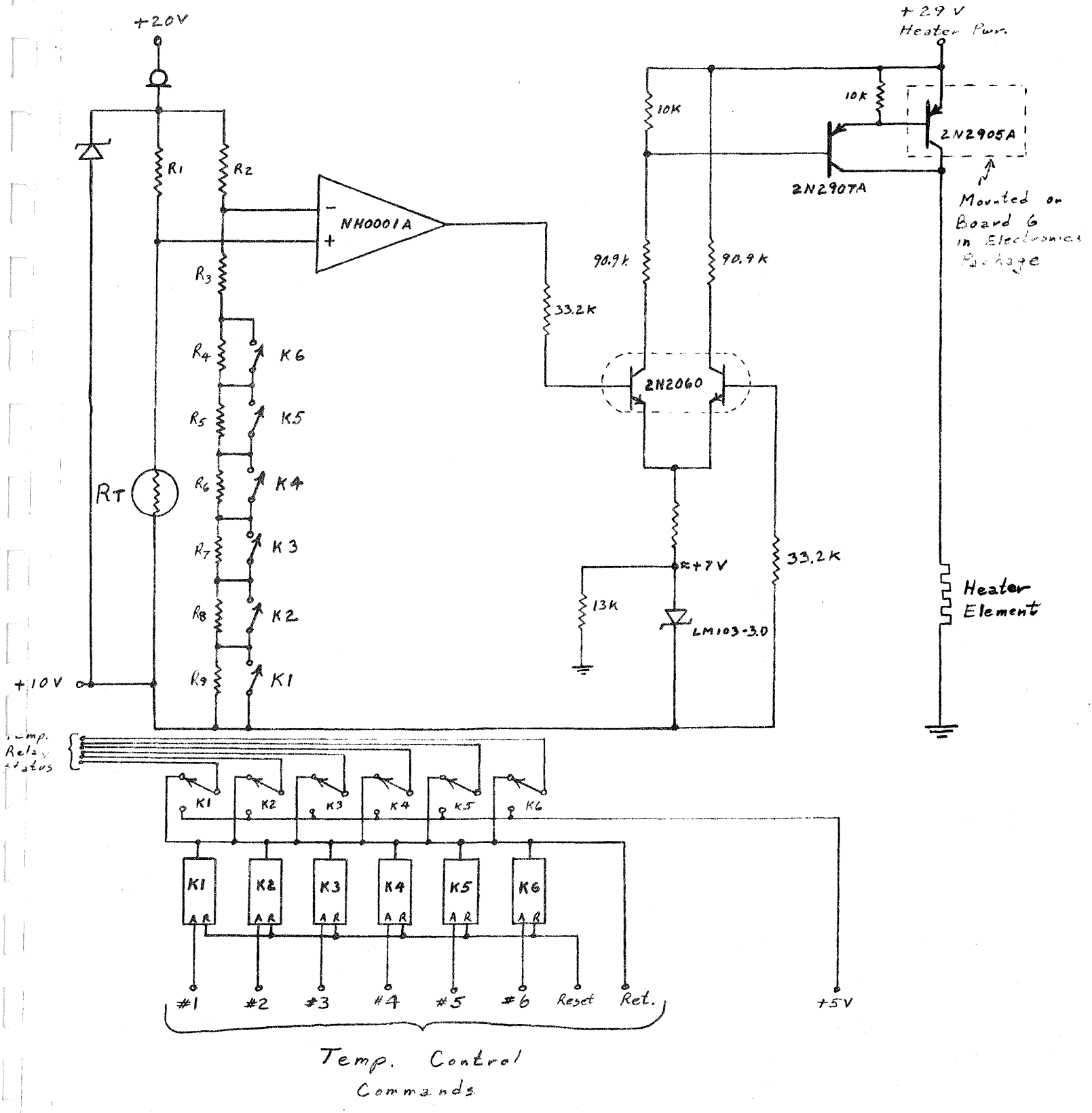


Figure 13-3 Heater Box Heater Controller (Simplified Schematic)