



**Aerospace
Systems Division**

FAIRCHILD FLATPACK
METALIZATION EFFECT ON EASEP

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EATM-65	
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DATE 20 March 1969	

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1.0 INTRODUCTION

The purpose of this EATM is to document the results of a special reliability assessment test which was performed to determine to what extent the internal metalization problem reported in ATM 806 would have on Fairchild LPDTL integrated circuits in the EASEP environment.

The results of ATM 806 in themselves were not completely adequate to determine this due to the difference in severity of environments to be experienced by the ALSEP system and the EASEP system and the difference in definition of a system failure for each program.

The ALSEP system will be a continuous operating system required to perform during lunar day and night. The main station electronic system will be exposed to a moderate temperature environment of a maximum of $+158^{\circ}\text{F}$ during lunar day and a minimum of -10°F during lunar night. The activity reported in ATM 806 addressed itself specifically to these conditions. The definition of failure for the ALSEP system would be the inability of the logic circuit to perform any one of its intended electrical functions at any temperature condition over the $+158^{\circ}\text{F}$ to -10°F range.

The EASEP system will not be a continuous operating system. Its power supply will be energized by solar cells which will be activated during lunar day time only, so operation will be limited to lunar day. The main station electronic system will be exposed to a moderate high temperature environment of $+140^{\circ}\text{F}$ average, to $+158^{\circ}\text{F}$ maximum. The low temperature environmental extreme will be severe to a minimum of -65°F , which will be experienced during lunar night. The electronics will have to survive this condition to be able to operate during the next lunar day period.

The definition of system failure for the EASEP system is quite different from that of the ALSEP system. The inability of the logic circuit to perform any one of its intended electrical functions during lunar day time temperatures only is considered an EASEP system failure.

2.0 SUMMARY

The products utilized for this investigation were those used in the earlier activity reported in ATM 806. A total of one hundred and fifty-six (156) devices were cycled for thirty-six cycles down to a -65°F temperature. A go/no go pulsed electrical functional test



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was performed on each device after each completed cycle.

Two devices produced system failures at +78°F during the investigation. Both were flip-flop devices (SL3538-4) and resulted in single failures during five (5) of the thirty-six (36) cycles. The failures occurred after cycle numbers 4, 27, 28, 33 and 34. The failed devices became operational while being tested during cycle numbers 4, 27 and 28 and would be operational at temperature above +78°F. No +78°F failures (system failures) of the LPDTL gate devices (SL3539-4 and SL3540-4) were detected during the investigation.

A conservative observation derived from these results is that the reliability of the EASEP system will be degraded at thermal base plate temperatures below +78°F and that operation above this temperature and up to +158°F will not result in alteration of the EASEP system reliability.

The EASEP system operation schedule should be altered to require that the "warm-up" time period be extended to allow the thermal base plate temperature to reach +78°F prior to system's use.

3.0 DISCUSSION

It was necessary to utilize products which represented the devices incorporated in the EASEP equipment. The only products available were those which had been used in the investigation reported in ATM 806. The devices were initially tested at -10°F prior to beginning this investigation to determine if additional failures had occurred since the activity reported in ATM 806. No additional failures were detected during this initial test. The identification of device types and quantities follows:

<u>QTY</u>	<u>ITEM DESCRIPTION</u>	<u>LOT CODE</u>
52	9040 flip-flop (SL3538-4)	6645
52	9041 gates (SL3539-4)	6633
52	9042 gates (SL3540-4)	6652
<u>156</u>	Total	

The test methods employed during this investigation consisted of a go/no go pulsed test technique which was capable of detecting malfunction of any functional characteristic of each device. Figures A-1 and A-2 of Appendix A are electrical schematics of the test



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circuits used. This test system comprised a sem-automated tester capable of accurate and rapid test measurements of device quantities up to fifty-two (52) pieces at one time.

The investigation began with a six (6) cycle test plan. A test cycle consisted of varying the temperature on the devices up to $+158^{\circ}\text{F}$, then down to -65°F and back to $+78^{\circ}\text{F}$ (room temperature). The profile of the cycle was not controlled since it was not feasible to attempt to duplicate a lunar temperature cycle due to the extremely slow rate of temperature change and extremely long time durations associated with the cycle. NASA (Goddard) has indicated in contacts with them that the time elements of the cycle contribute nothing to the metalization problem and that only the low temperature extreme and the total number of cycles are determining factors in the cause of metalization degradation. The cycle used in this investigation is shown in Figure 1.

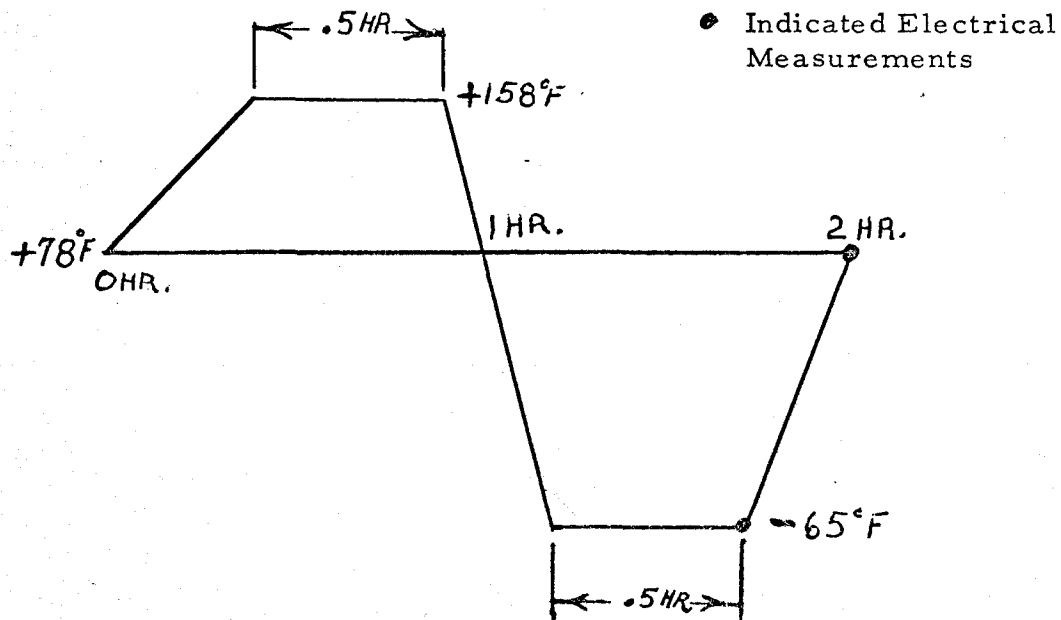


FIGURE 1

TEMPERATURE CYCLE

The dwell times at $+158^{\circ}\text{F}$ and -65°F were maintained for 30 minutes minimum.



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TEMPERATURE	CYCLE #	6	12	18	24	30	36
S J M M M 4	>78°F						03 03
	+78°F	07				03 03	03 03
	-65°F	17 17 13					
S J M M M 4	>78°F						
	+78°F						
	-65°F	44 44 45	44 44 45	44 44 45	44 44 45	44 44 45	
S J M M M 4	>78°F						
	+78°F						
	-65°F		02 09				

FIGURE 2

TEST RESULT SUMMARY

The numbers shown in the boxes are the actual test serial numbers which failed.

One flip-flop device, S/N 07, failed during the first six cycles at +78°F, but became operational as it was being observed. Several -65°F failures were detected, but all became operational before +78°F was reached. The gate device, S/N 445, failed repeatedly at -65°F after every cycle but never was observed or failed at +78°F even beyond six cycles.



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Figure 2 also shows additional cycles which were performed after completion of the six (6) cycles originally planned. This was done to obtain additional test data to enable the preparation of a statistical treatment. This treatment is contained in Appendix B.

The test procedure was revised during the additional thirty (30) cycles to achieve the additional cycles as quickly as possible.

The elimination of the $+78^{\circ}\text{F}$ to $+158^{\circ}\text{F}$ temperature excursion during each cycle and the -65°F electrical test after each cycle allowed for the accumulation of data at nearly three times the original rate. NASA (Goddard) adopted the approach of cycling from $+78^{\circ}\text{F}$ to the low temperature limit in their investigations to obtain data as quickly as possible. They indicate that the positive temperature excursion does not effect the metalization problem. It was therefore omitted from the additional cycling. The electrical test at -65°F was performed only as a means to determine if devices which malfunction at -65°F would become operational at $+78^{\circ}\text{F}$. The EASEP system will not be required to function during lunar night (-65°F) since the solar cells will not supply power until the sun rises. Elimination of the -65°F test does not effect the failure data.

One device produced a system failure during the last thirty cycles. The flip-flop device, S/N 03, appeared as a system failure at $+78^{\circ}\text{F}$ after the twenty-seventh (27th) and twenty-eighth (28th) cycles. On these occasions, the device became operational as the failure was being observed. The device operated satisfactorily after cycles 29, 30, 31 and 32. It again failed at $+78^{\circ}\text{F}$ after cycles thirty-three (33) and thirty-four (34) and did not become operational until a higher temperature was achieved. The device did not experience failure again after each of the last two cycles. It appeared, however, that this device was becoming more susceptible to failure at these later cycles.

4.0

RESULTS AND CONCLUSIONS

Figure 2 reveals that $+78^{\circ}\text{F}$ is apparently a temperature limit at which the metalization problem begins to adversely effect the reliability of the Fairchild LPDTL circuit devices. This is derived from the fact that of two device failures at $+78^{\circ}\text{F}$, both were observed as operational shortly after being detected failed at $+78^{\circ}\text{F}$ at least through thirty-two (32) cycles,



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The first six (6) cycles reveal that several other devices experienced failure at -65°F , but that this did not relate to their operation at $+78^{\circ}\text{F}$. It is probable that many more devices became non-operational at -65°F during the ensuing cycles, but remained operational at $+78^{\circ}\text{F}$.

NASA (Goddard) and others have also reported similar findings. Their investigations have shown that although devices fail at low temperature, they remain operational at higher temperatures. This experience is customary of any type of fractured connection.

The conclusion reached from these results is that the metalization problem associated with the Fairchild LPDTL product degrades the reliable operation of such devices at low temperatures. It has been observed that no devices failed continuously at $+78^{\circ}\text{F}$ for at least thirty-two (32) cycles, but that failure to operate at that temperature was experienced for short periods of time. This would tend to indicate that $+78^{\circ}\text{F}$ is a limit at which operation can become impaired. It is concluded that operation of the EASEP equipment at temperatures between $+78^{\circ}\text{F}$ and $+158^{\circ}\text{F}$ will not effect the reliability of the system. Operation at temperatures below $+78^{\circ}\text{F}$ might result in reduced system reliability.

It is recommended that the operational period for the EASEP system be limited to thermal plate temperatures between $+78^{\circ}\text{F}$ and $+158^{\circ}\text{F}$ so that system reliability will be unaltered due to the low temperature metalization problem in the Fairchild LPDTL integrated circuits.

Should requirements for early day data override this recommendation, an awareness of possible errors in this first light data with probable corrections later in the lunar day, should be understood.

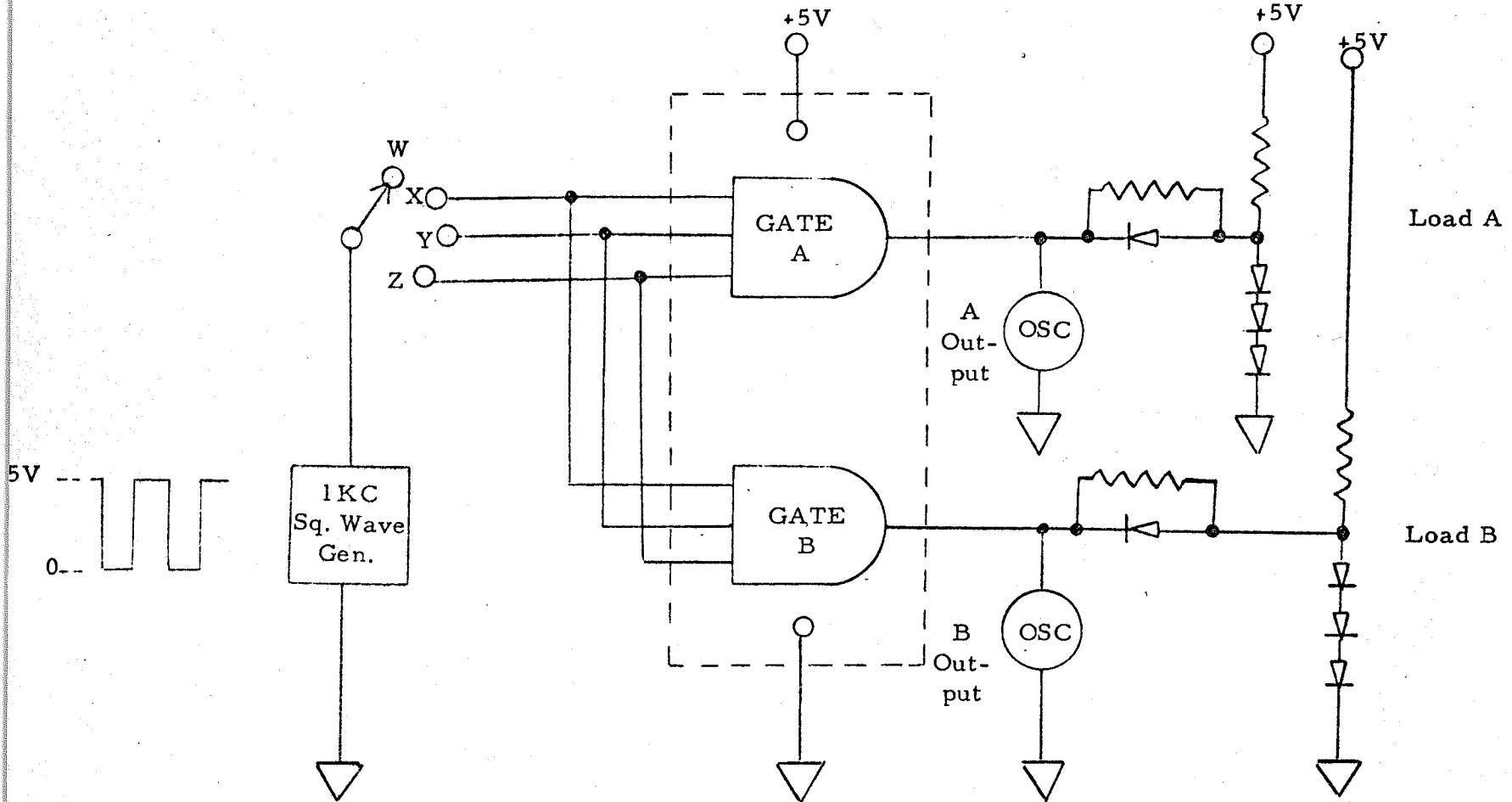


FIGURE A-1

SL 3539 and SL 3540 TEST CIRCUITS

APPENDIX A

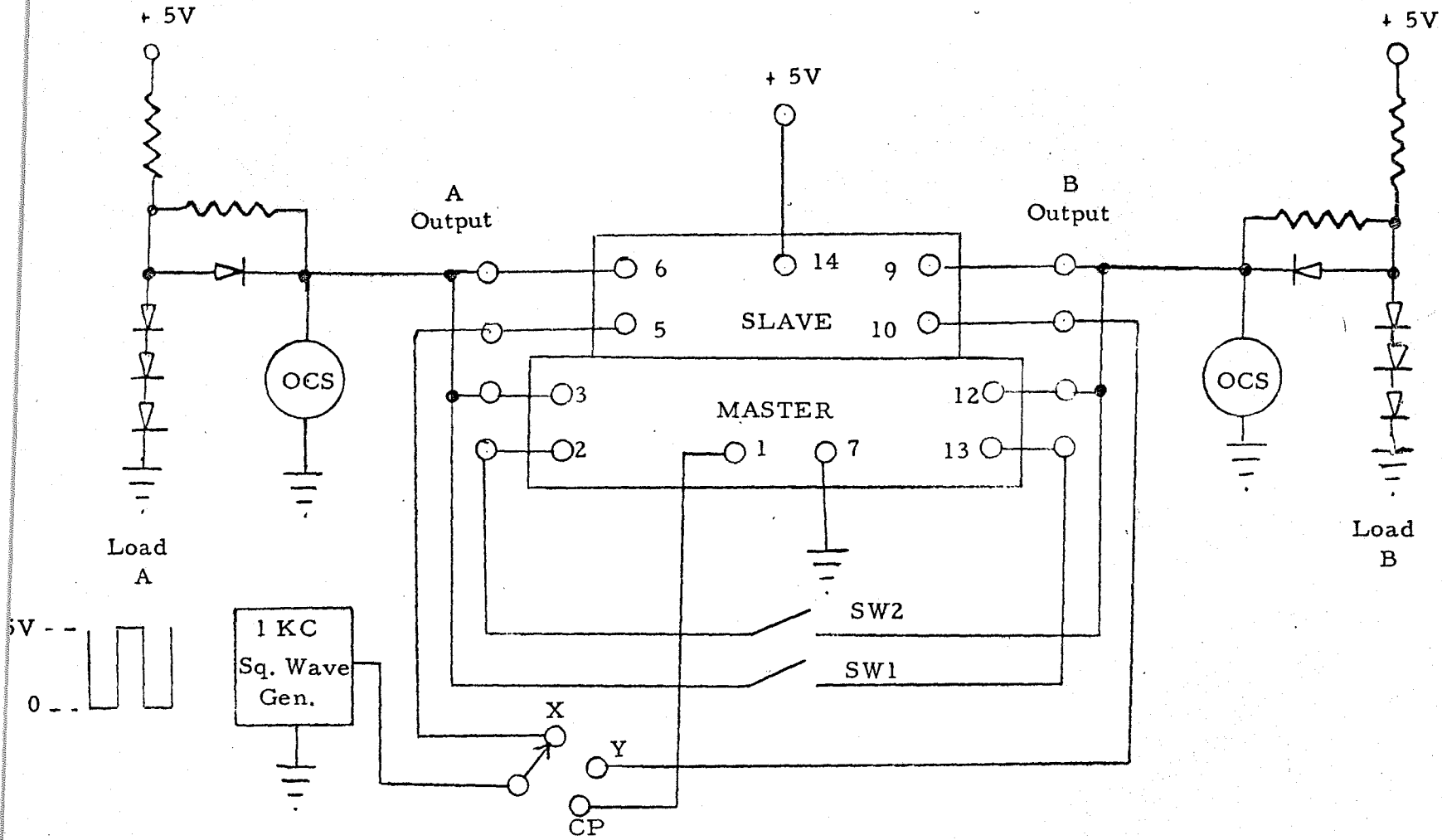


FIGURE A-2

APPENDIX B

STATISTICAL TREATMENT FOR FAILURE RATE DETERMINATION

Contained within this appendix is a summary of the preliminary analysis of the flatpack failure rate as adjudged from test data collected per this study.

Basic methodology utilized in derivation of applicable failure rate data for this failure mode was computation of the cumulative hazard¹ associated with these flatpacks based on the following precepts:

1. Failure occurring at +78°F only were counted for this analysis in that all parts failing initial tests at -65°F subsequently operated satisfactorily at +78°F. Furthermore, that part which failed at a higher temperature than +78°F (SL3538-4, S/N 03) had previously failed at +78°F (Note Item 2 below.)
2. Only initial failures at +78°F were counted. This was accomplished in that a Weibull analysis of the one part showing repetitive failures at this temperature indicated these failures to be of the wearout type; the conclusion being that only mean cycles to failure is applicable as a figure of merit for these parts.
3. Cumulative hazard was computed on the basis of the exponential distribution for those two parts that did fail at +78°F in that Weibull analysis data indicated this approach to be of a more conservative nature than would otherwise be existant if a decreasing failure rate were assumed to exist.
4. Compilation of cumulative hazard data was based on the full complement of 156 flatpacks subjected to test inasmuch as even though only SL 3538-4 flatpacks failed at +78°F, other devices failed during the initial six (6) cycles of test data accumulated at -65°F.

1. Reference: Hazard Plotting for Incomplete Failure Data, Wayne Nelson, Published in Journal of Quality Technology, Volume 1, No. 1, January 1969.



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Based on these precepts, the applicable cumulative hazard data from these tests may be summarized as follows:

TABLE B-1

Flatpack Failure Data and Hazard Calculations

<u>Sample No. *</u>	<u>Cycles</u>	<u>Hazard</u>	<u>Cumulative Hazard</u>	<u>Remarks</u>
1	4	0.641%	0.641%	SL 3538-4, S/N A-17
2	27	0.645%	1.286%	SL 3538-4, S/N -03
3-156	36	--	--	Remaining samples passed test at +78°F

As described by Mr. Nelson in the listed reference, to attain the estimated mean cycles to failure, it is necessary to derive the cycles to failure at the 100% cumulative hazard point. This was accomplished by use of the formula:

$$Y = ax - b \quad (\text{Equation B-1})$$

in which

- Y = cumulative hazard (Total)
- a = cumulative hazard/cycle/part
- b = initial cumulative hazard/part
- x = cycles to failure

By algebraic derivation, $a = 0.02804\%$ and $b = 0.529\%$. Thus, with $y = 100\%$, $x = 3547.5 =$ mean cycles to failure. As a result, the assumed failure rate for these flatpacks is 28.2 %/1000 cycles.

*In sequence of failures.