Bendix
Aerospace
Systems Division

ALSEP Array E Multilayer
Printed Circuit Board
Source Qualification Test Plan

NO.	REV. NO.
ATM 988	

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DATE

This document provides a test plan for source or manufacturer qualification in the manufacture and supply of multilayer printed circuit system(s) with plated through holes.

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1.0 SCOPE

This test plan describes the necessary requirements for source qualification in the fabrication of multilayer printed circuit systems with plated-through holes in accordance with JPL Spec No. FS 505789A.

2.0 APPLICABLE DOCUMENTS

The following documents form a part of this test plan to the extent specified herein.

JPL Spec. No. FS 505789A, Detailed Specification for Fabrication of Multilayer Printed System with Plated-through Holes

Institute of Printed Circuits Standard Specification IPC-ML-950A, Performance Specification for Multilayer Printed Wiring Boards

3.0 TEST SPECIMENS

The test specimens shall be qualification test production board samples, patterned in accordance with IPC-ML-950A, or to the most complex board configuration to be supplied.

4.0 OBJECTIVES

The objectives of this qualification test plan are to verify that reproduction multilayer printed wiring boards meet the Supplier Qualification requirements of JPL Specification No. FS 505789A.

5.0 TEST SEQUENCE

The Qualification Test shall be performed in accordance with test procedures specified herein. Samples, identified as A through H (eight specimens) shall be tested as shown in Table 1 and referenced paragraphs of this document.

5.1 Tests

The following tests are to be performed in the sequence shown and per assignments of specimens as given in Table 1.

5.1.1 Visual and Dimensional Examination

Examine in accordance with requirements and tests of JPL Spec No. FS505789A, 3.3, 3.4, 4.4.1.

5.1.2 Warp and Twist

Measure warp and twist in accordance with JPL Spec FS505789A, 3.4.15. Warp or twist shall not exceed one percent (1%) when using entire qualification specimens.

5.1.3 Plating Adhesion

Plating adhesion testing shall be performed in accordance with requirements and test qualification requirements of ICP-ML-950A, 3.4.1.3 and 4.4.5, respectively.

5.1.4 Electrical Checkout

Each plated through hole's electrical continuity shall be tested using a 6 volt dry cell buzzer system or equivalent.

5.1.5 Interconnection Resistance

Interconnection resistance shall be tested in accordance with 3.4.1.10 and 4.4.9 of IPC-ML-950A.

5.1.6 Insulation Resistance

Insulation resistance shall be tested in accordance with 3.7.5 and 4.6.4 of JPL Specification FS505789A.

5.1.7 Preconditioning

Bake test specimens in accordance with the temperatures, periods and relative humidity values given in JPL Specification FS505789A, 4.5.8.

5.1.8 Heat Resistance

Heat resistance shall be determined by a hot oil test in accordance with 3.6.7 and 4.5.7, JPL Spec. FS505789A.

5.1.9 Warp and Twist

Test in accordance with 5.1.2 herein.

5.1.10 Internal Shorts

Determination of internal shorts (less than 500 megohm resistance) shall be in accordance with 3.7.3 and 4.6.2 of JPL Spec. FS505789A.

5.1.11 Cross Sectioning

Cross sectioning of multilayer printed circuit boards shall be accomplished in accordance with JPL Specification FS 505789A, 3.4 4.4.2 and 6.3. Etch-back shall be in accordance withthe requirements of JPL ES 505789A, 3.4.11.

5.1.12 (See Test 12 Note, Table 1 herein).

5.1.13 Interconnection Resistance

Interconnection resistance shall meet the requirements of JPL Spec. FS505789A, 3.7.6 and 4.6.5, using equipment and methods as provided in IPC-ML-950A, 4.4.9.

5.1.14 Thermal Shock - Temperature Cycling

Thermal shock - temperature cycling shall be conducted in accordance with JPL Spec. FS505789A, 4.6.6 and the requirements of 3.7.7 of this same specification.

5.1.15 Interconnection Resistance

Test in accordance with 5.1.13 above.

5.1.16 Moisture Resistance

Moisture resistance shall be tested in accordance with the requirements of JPL Spec. FS505789A, 3.7.8 and 4.6.7.

5.1.17 Insulation Resistance

Test in accordance with 5.1.6 herein.

5.1.18 Current Carrying Capacity

Current carrying capacities shall be in accordance with the requirements of JPL Spec. FS505789A, 3.7.2 and 4.6.1.

5.1.19 Final Tests

Fourteen tests on seven speciments are given in Test 19, Table 1 herein. Cross sectioning shall be accomplished as required in 5.1.11 herein. Insulation resistance shall be in accordance with 5.1.6 herein. Dielectric withstanding voltage shall be in accordance with the requirements and testing procedures as provided in JPL Spec. FS505789A, 3.7.4 and 4.6.3 respectively. Flexural strength shall be in accordance with the requirements and testing procedures as provided in JPL Spec. FS505789A, 3.6.4 and 4.5.4 respectively. Water absorption, flammability, PTH bond strength and solderability shall be conducted in accordance with the requirements and tests designated in JPL Spec. FS505789A, Table III, Test 19, last four lines and related paragraphs referenced therein.

6.0 TEST REPORT AND ANALYSIS

A test analysis shall be provided, stating the satisfactory or unsatisfactory results of the tests for supplier qualification with highlights of marginal and out of tolerance results obtained during the tests and post test examinations and measurements. The test reports or test report summaries, documenting the multilayer printed circuit board performance shall be appended to the test analysis and be amply referenced throughout the test analysis. This analysis/test report shall be retained for 3 years by the supplier and be presented to the purchasing agency upon request from that agency.

TABLE I

Test	Paragraph	Specimen(s)*	Test Description
1	5.1.1	all	Visual and Dimensional Examination
2	5.1.2	all	Warp and Twist
3	5.1.3	B	Plating Adhesion
4	5.1.4	all	Electrical Checkout
5	5.1.5	G	Interconnection Resistance
6	5.1.6	A&H	Insulation Resistance
7	5.1.7	all	Precondition
8	5.1.8	all	Heat Resistance
9	5.1.9	all	Warp and Twist
10	5.1.10	B	Internal Shorts
11	5.1.11	B	Cross Sectioning (as applicable)
12	Cut out Specimens G and H, test as a unit per tests 13 through 19, in this table. Cut out other specimens as required in test 19 and test individually as required.		
13	5.1.13	G	Interconnection Resistance
14	5.1.14	G&H	Thermal Shock - Temperature Cycling
15	5.1.15	G	Interconnection Resistance
16	5.1.16	G&H	Moisture Resistance
17	5.1.17	H	Insulation Resistance
18	5.1.18	G	Current Carrying Capacity
19	5.1.19	G	Cross Sectioning
		A	Insulation Resistance
		A	Dielectric Withstanding Voltage
		C	Flexural Strength
		D	Water Absorption
		E	Flammability
		F	PTH (plated through holes) Bond Strength
		F	Solderability

*Specimens A through H board areas shall be not less than nine (9) square inches as derived from sectioning larger board(s). The sections shall be adequately marked for tests 1 through 11 and not physically sectioned until test 12 above.