ARRAY E

COMMAND DECODER

FUNCTIONAL DESCRIPTION

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1.0 INTRODUCTION

This ATM introduces a preliminary circuit and logic description of one redundant portion of the ALSEP Command Decoder. The description is presented in a board by board format in the direction of signal flow. Figure 1 shows the block diagram of one side of the redundant portion of the Command Decoder, and also of the non-redundant (back-up) functions on the Command Sequencer board.

The logical flow of a ground command is from the receiver to the Data Demodulator, where it is converted into digital form and passed to the Control Logic and then to the Decode Gate board. The form of this data is three seven bit words, the first being the ALSEP address, the second the command complement for parity checking purposes, and the third word is the command. The Command Sequencer board provides the back-up functions of generating the repeated commands, the uplink switch-over circuit, and the ripple-off circuit.

2.0 DATA DEMODULATOR

The Data Demodulator circuit converts biphase baseband data from the Command Receiver into "Non Return to Zero" (NRZ) digital data and also provides uplink clock and threshold signals for the control logic portion of the Command Decoder.

The unit is designed to accept a composite waveform which is the sum of a 1 KHz clock and a 2 KHz data subcarrier. The 2 KHz subcarrier is biphase modulated by a 1000 bit/second data stream.

The block diagram of the Data Demodulator is shown in Figure 2. This shows the three basic sections of the unit:

a. Phase Lock Loop and Clock Generator
b. Data Detector
c. Threshold circuit.

2.1 PHASE LOCK LOOP

The Phase Lock Loop (PLL) section provides the signals both to detect the data and clock it out to the Command Register in the Control Logic Section by locking to the 1 KHz uplink clock generated at the ground station.

The phase lock loop contains a voltage controlled oscillator with a free running frequency of 8 KHz. The VCO output is counted down in a four stage ring counter to generate 4 phases of a 1 KHz square wave. The phase at 90° to the incoming 1 KHz signal drives the phase sensitive rectifier(PSR) switches, producing an error signal proportional to the phase error between the incoming 1 KHz and the generated 1 KHz. This error signal, filtered and amplified, is used to drive the VCO to the phase lock condition. The other phases of the 1 KHz clock are gated together to produce the control logic clocks and provide 2 KHz signals for the data detector.

2.2 DATA DETECTOR

The data detector consists of two detection chains, one to detect "1" bits and the other to detect "0" bits. Each chain comprises a PSR followed by an "integrate and dump" circuit and a comparator. In each chain the incoming audio is sampled in the PSR at either the first and third or the second and fourth quarters of a bit period, by the 2 KHz signals generated in the phase lock loop. The output of the PSR has a net positive or negative voltage depending on whether the bit is a "1" or a "0". This output is applied to a capacitor which integrates this voltage, for the period of one bit, after which the capacitor charge is dumped through a switch to ground. The output of the integrate and dump circuit is compared to a fixed threshold voltage at the comparator and if this voltage is exceeded then the comparator switches, generating a logic "1". The comparators are connected to give a logic "1" output when a valid bit one is detected in the "1" chain and when a good bit zero is detected in the "0" chain. The comparator outputs are clocked into the data flip flop by a short pulse generated near the end of each bit. Thus, NRZ data is obtained from the data flip flop, delayed by one bit from the base-band data.

2.3 THRESHOLD CIRCUITS

The threshold circuits are in two sections. Firstly, the analog threshold, described in paragraph 2.2, which ensures that output of the integrate and dump circuit is large enough before the comparators can produce data.

Secondly, the digital threshold circuit which ensures that at least four valid data bits must be produced before the NRZ data is allowed into the Command Register in the Control Logic. This is accomplished by comparing the data comparator outputs in an "exclusive or" gate which produces logic "1" signals only if the outputs are complementary i.e. valid data. The "exclusive or" output is shifted through a 4 stage register by the data flip flop clock, and the outputs of each stage of the register are gated such that a logic "1" signal is produced only if all the outputs are high, i.e., four valid bits have been successively detected. This gate output is the digital threshold signal, and it is used to inhibit the data flip flop and also to reset the control logic, should a data dropout occur.

3.0 CONTROL LOGIC

The Control Logic consists of an eight bit shift register, two counters, and reset circuitry, see Fig. 3. The shift register (Command Register) has the demodulated split-phase data stream from the ground station passing through it at the uplink data rate of 1 KHz. A gate constantly samples the first seven bits of the shift register for the address of the particular ALSEP (1101001 for Array E). The connections from the shift register to the address recognition gate is through a mother-board matrix, enabling different addresses to be selected with no printed circuit changes.

Once an address is recognized, a timing sequence is initiated. The first counter produces one pulse output for every seven clock pulses input (divide by 7). This output then clocks a binary counter which acts as master control for the timing. After address recognition, the next seven pulses shift the command complement into the last seven bits of the shift register.

The binary counter, now in the state 001, ensures that the next seven bits of data (the command) clocked in are checked for parity. An "exclusive or" gate sensing the first and last bits of the shift register performs a parity check on each bit of the command complement and the corresponding bit of the command. Bad parity will set the parity memory.

The next three states of the binary counter (21 mS) define the command execute sequence by setting a latch, and also inhibit the clock pulses to the shift register by means of another latch. At this time, the command will be present in the last seven bits of the shift register.

The command sequence pulse is gated with the parity memory to produce a command execute pulse, causing the command line corresponding to the command code in the shift register to be energized. This will only occur if the parity check was good.

After the command has been executed, a logic signal VWEZP is sent to the Data Processor by a timing latch, causing a data demand signal DDIZP to be sent back to the command decoder during the interval of the next Command Verification Word in the downlink frame. A dual flip flop gates out the first two downlink shift pulses generated in the Data Processor, inserting two filler bits, and allows the next eight to shift the contents of the shift register to the Data Processor as the signal EDIZP. The eighth bit shifted out is set to a 1 for good parity, and to 0 for bad parity. Of the 10 bits in the CVW recieved by the ground station, the first two are filler bits, and identical to the most significant bit of the command word, which occupies bits 3 to 9. The tenth bit is the parity check bit, with a 1 indicating good parity and that the command was executed.

A master reset is completed at the end of the data demand pulse by using the phase relation between data demand and CWEZP, a Data Processor generated clock, to reset all latches to the address search mode. The two counters that control the timing are not reset by this master reset, but are reset to 000 when an address is recognized.

When the Central Station is commanded into the High Data Rate mode, no data demands are generated by the Data Processor and an alternative means of master reset must be used. A latch is used to generate the high data rate command HKFZN sent to the Data Processor, and also to cause the last 1 mS of the 21 mS command execute period to be used as a master rest. This causes all commands to be 20 mS long while the Central Station is operating in the High Data Rate mode.

4.0 DECODE GATES

The decode gate matrix decodes a seven bit binary command into individual command lines. A command execute pulse, CEXAN, is used to create the correct command pulse length.

The decoding takes place in two levels. The first level creates outputs from all combinations of the first four bits (16) and from all combinations of the remaining three bits (8). This is accomplished with four-input gates, with the fourth input of the group of eight used for the command execute pulse.

The output decoding is carried out with two input gates, all having inputs associated with each of the two groups of first level gates (see Figure 4). This ensures each output is dependent on the states of all seven input bits and on the command execute pulse.

One hundred and four commands of a possible 128 are decoded, with resistors provided in 53 outputs for rise time control. The capacitors for this control are provided on the Control Logic board. The output waveform is a negative pulse of 20 ± 2 mS duration.

5.0 REPEATED COMMAND SEQUENCER

The Command Sequencer consists of a free running binary counter with decoding logic wired to Experiment Calibrate command lines (Fig. 5). The sequencer also functions as an uplink switch-over timer to ensure a switch from one uplink chain to the other in case of an uplink failure.

The clock for the counter is the 90th frame mark, NFIZP, a 118 μS pulse appearing every 54 seconds, generated within the Data Processor. The repeated commands are generated by sensing a binary count on the first 10 bits of the binary counter. Since only the 10 least significant bits of the counter are sensed, they will repeat themselves within a period of approximately 15.4 hours. Each count will last for one clock period (i.e., 54 seconds), so an 18.8 mS strobe pulse is generated to produce the correct period for a command. This strobe pulse is started by the 90th frame mark and is ended by the start of control word three, THRZN, also obtained from the Data Processor.

Once the commands are generated, they are "OR'd" with the experiment calibrate command lines in the redundant section of the command sequencer. Also within this redundant section is an "enable/inhibit repeated commands" flip flop which, by means of two commands, lets the ground user of ALSEP decide whether the repeated calibrate commands should be provided to the experiments or not. This inhibit feature also permits the repeated command sequencer to be disabled in case of a failure in any of the non-redundant circuitry.

The three repeated commands are generated with intervals of seven minutes but since the LEAM experiment requires two calibrate pulses, the PSE is also ORed into the LEAM calibrate command line to produce two pulses seven minutes apart. This gives the following order of experiment calibrate commands every 15.4 hours: PSE and LEAM 1, LEAM 2, LSM.

The 12 bit binary counter also acts as the uplink switch-over timer by producing a 19 mS strobed switch-over command every 61.8 hours. A command received from the ground, "delay uplink switch", will inhibit this switch-over, but it must have been received in the 59.3 hours previous to the switch-over command. In normal use, it is anticipated that this command will be sent at least once every two days, causing the uplink chain to remain permanently in one of its redundant states. However, should this uplink chain fail, the "delay uplink switch" command will not be received, and the strobed switch-over command will cause a change of uplink chains. A command is also provided to cause an immediate change of uplinks for system test purposes.

6.0 RIPPLE-OFF CIRCUIT

The Ripple-Off circuit consists of an 8-bit binary counter and decoding gates producing the commands. The counter is clocked by the CWE clock, a 1060 Hz clock generated within the Data Processor. The loss of a "Reserve Power" signal from the PCU causes seven power loads to be switched sequentially to standby after a predetermined length of time. This circuitry is incorporated on the Command Sequencer Board (Fig. 5).

The counter is set to a binary count of 7 by the Power On reset pulse. When the reserve power signal becomes a logic 0, the clock to the counter is enabled, and the count starts. If the reserve power line is still low when a count of 136 has been reached, an output lasting for 8 clock pulses will be generated on the first command line. If there is still a lack of reserve power each of the remaining six command lines will successively receive commands, all being 8 clock pulses long.

If the reserve power line should change back to a logic "1" during this sequence, the command being executed will remain for sufficient time to complete its period of 8 clock pulses. This is ensured by only resetting the counter and inhibiting the clock when a binary count of 111 exists in the first three stages of the binary counter.

Should the circuit ripple-off all seven outputs, the clock is inhibited by a second line which is driven by a gate sensing "1's" in the last two stages of the binary counter. Since a failure can occur in several places that could make this occur, this second inhibit is a stable state that can only be reset by a command sent from the ground. This feature, and the redundancy in the decode gates, ensures no single point failures on any of the logic output lines.

COMMAND DECODER

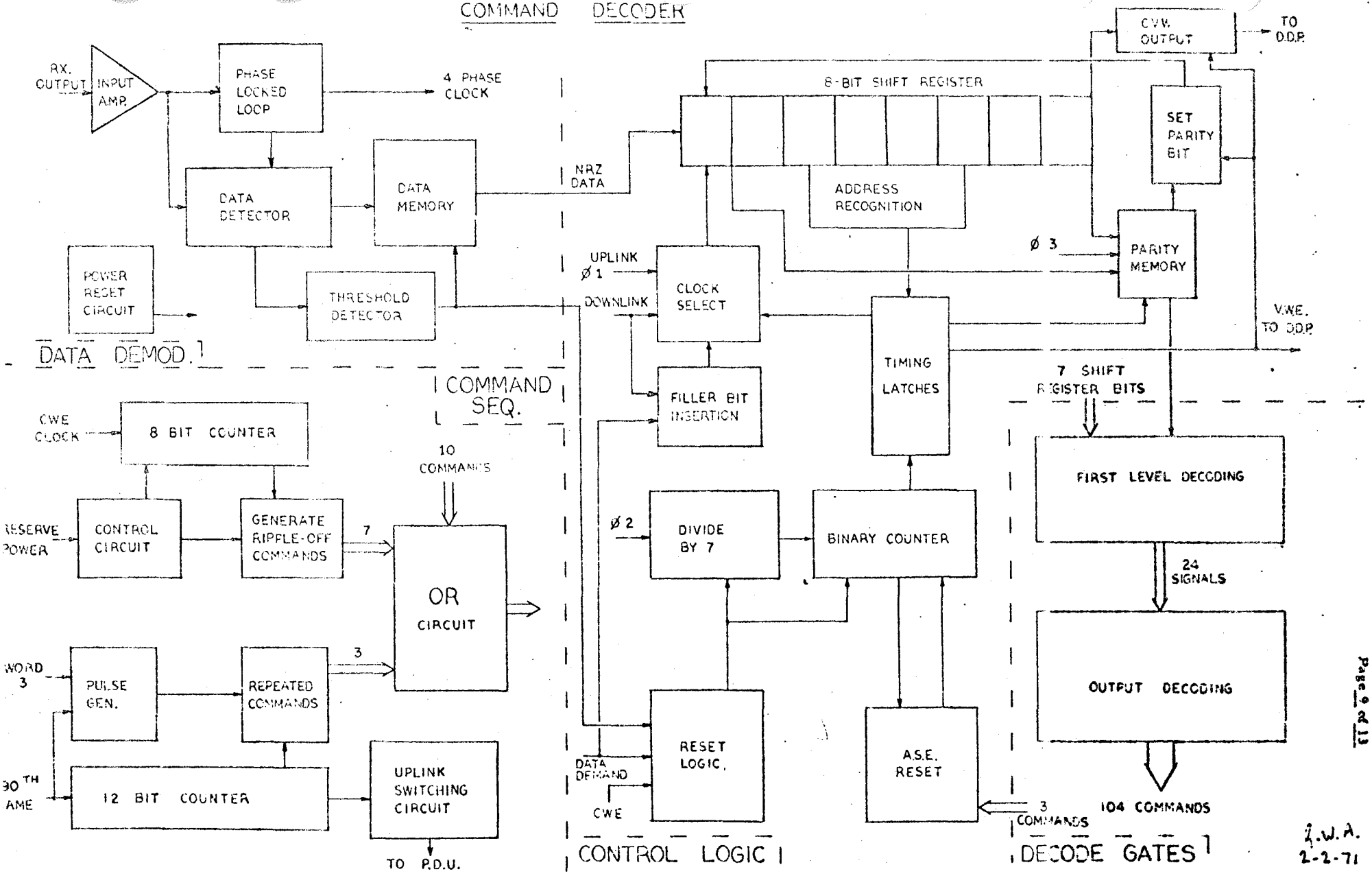

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FIG. 2

DATA DEMODULATOR - BLOCK DIAGRAM

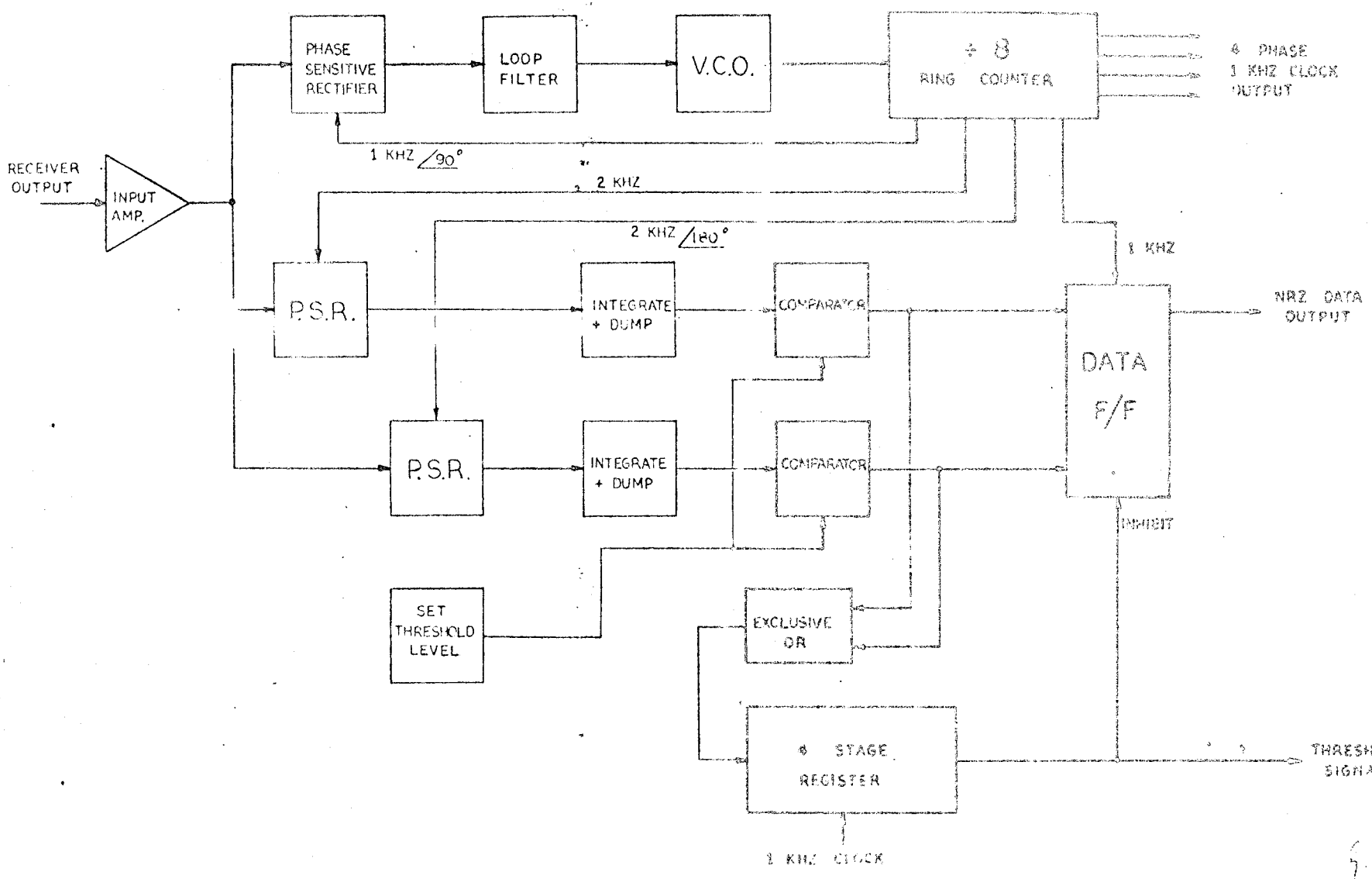

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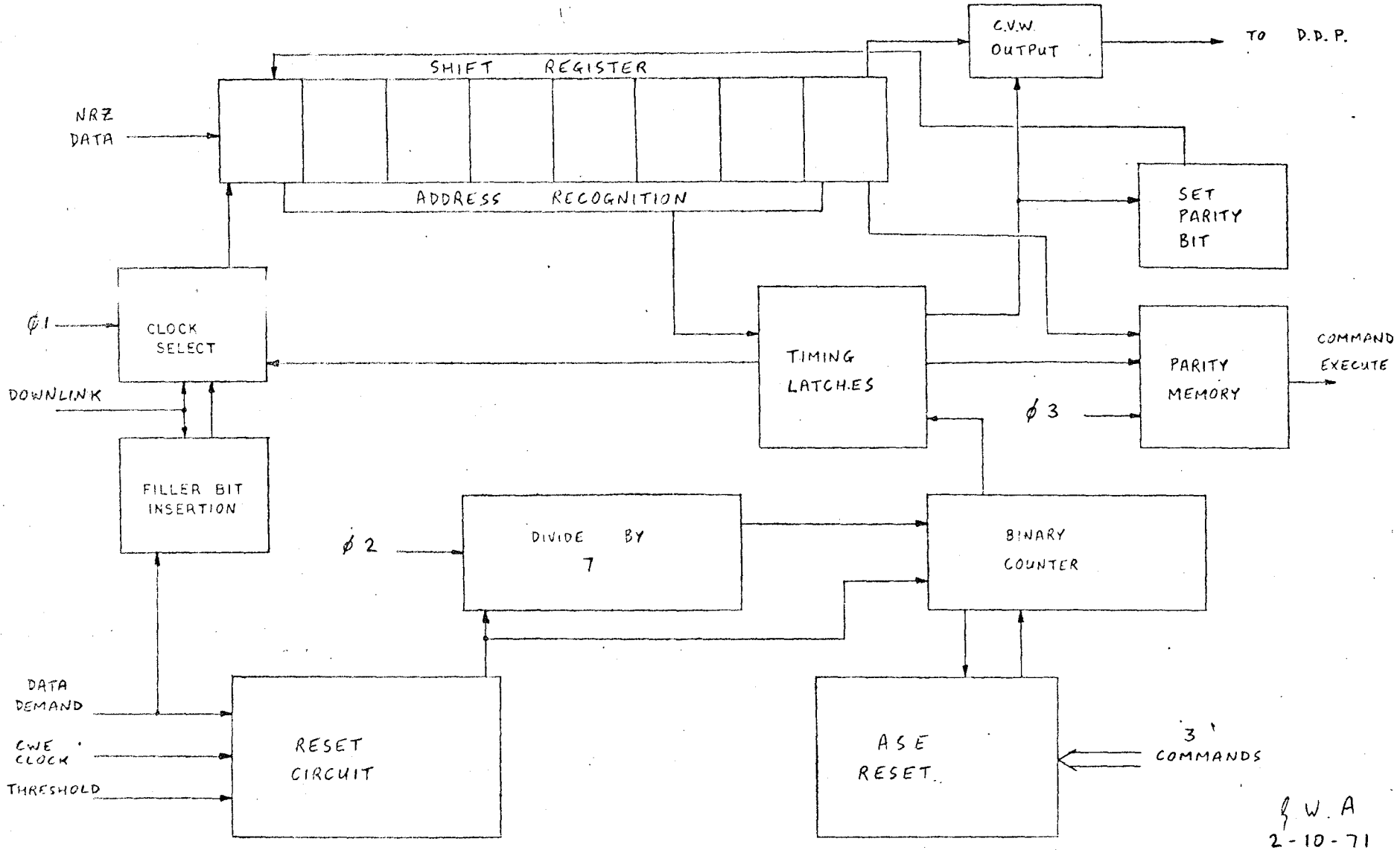
FIG. 3

CONTROL LOGIC



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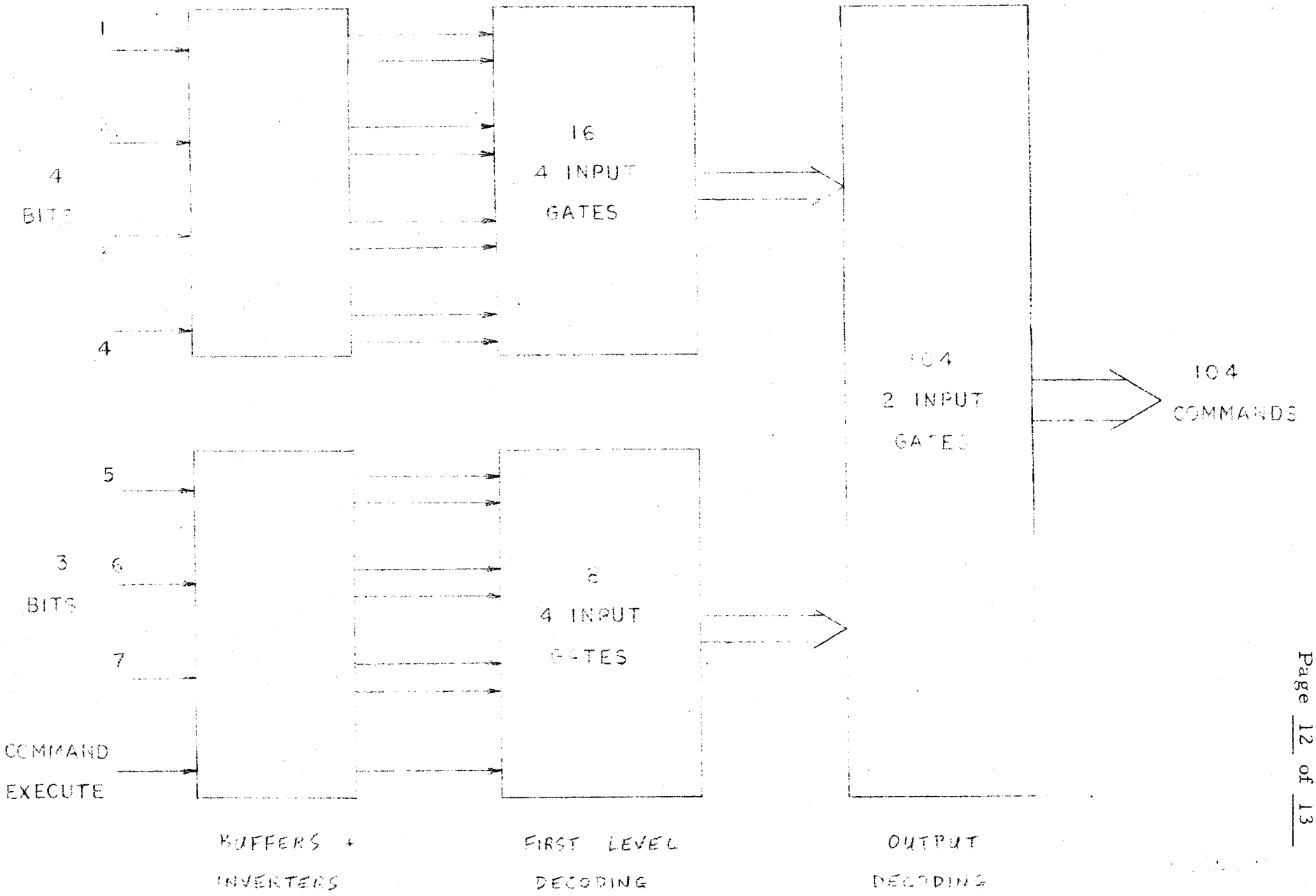
1
2
4
BITS
4
16
4 INPUT
GATES
104
2 INPUT
GATES
104
COMMANDS
5
6
7
3
BITS
8
4 INPUT
GATES
COMMAND
EXECUTE
BUFFERS +
INVERTERS
FIRST LEVEL
DECODING
OUTPUT
DECODING

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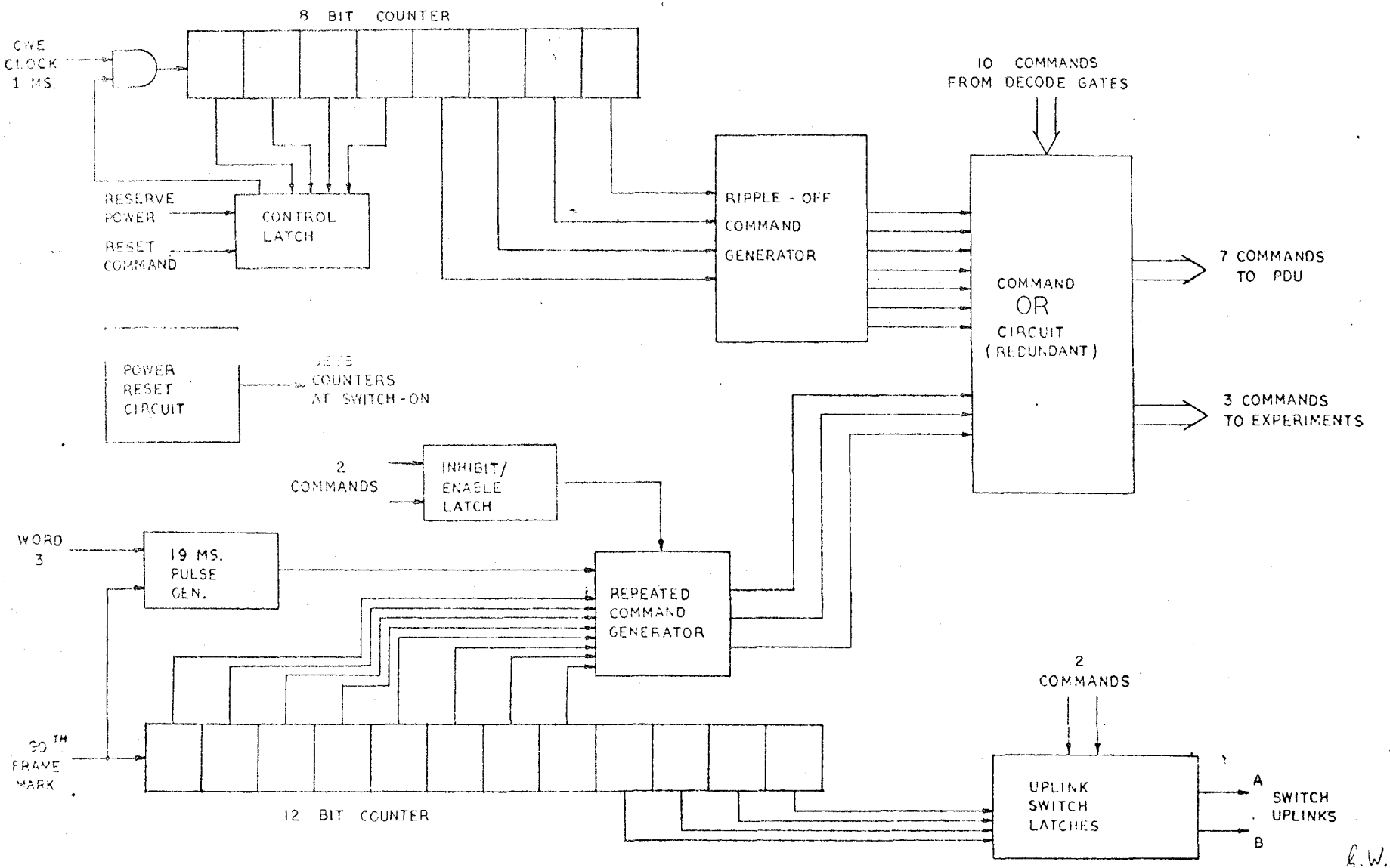
FIG. 5

COMMAND SEQUENCER



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